Final Project Report

on

DESIGN AND DEVELOPMENT OF 100-VA INTEGRATED STATIC INVERTER

For the Period

June 1966 through June 1967

Contract No. NAS8-11925

Control No. DCN 1-6-40-56195(2F), S3(1F)

Prepared by

TEXAS INSTRUMENTS INCORPORATED
Semiconductor-Components Division
P. O. Box 5012
Dallas, Texas 75222

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
George C. Marshall Space Flight Center
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ACKNOWLEDGEMENTS

J. P. Vergez, Program Manager

L. L. Glover, Circuit Design

L. A. Hahn, Power Device Design

ABSTRACT

The 100-VA direct-coupled inverter is a 28-volts-dc to three-phase, 400 Hz sine wave inverter that uses a unique matrix of power switches to achieve the desired step-approximated waveshapes. Because of the unique arrangement of power switches, no transformers are required in the inverter itself, thus eliminating the need for those components usually considered the largest and heaviest of all inverter components. The complete inverter does use one transformer, however, in the switching regulator portion.

Since funds were exhausted before development of the inverter was complete, this report summarizes the work accomplished through June 1967.

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SECTION I

HISTORY

In May 1965 the direct-coupled inverter approach was conceived by Paul Vergez of Texas Instruments. It was at this time that Texas Instruments had been awarded the developmental contract for three transformer coupled 75-VA inverters from NASA-Huntsville. As work progressed on the 75-VA inverters, TI independently continued developing the direct-coupled inverter approach until a preliminary 75-VA direct-coupled breadboard was evolved. The breadboard was submitted to NASA for evaluation in January 1966, after which NASA directed to TI an RFQ on two prototype 100-VA direct-coupled inverters. A TI proposal was submitted in February 1966. In addition to the two inverters, the development of several special transistors and fabrication of multichip transistor packages were proposed to minimize the size and weight requirements of the inverters

Specifically, it was proposed to develop a single chip Darlington PNP transistor, three of which were to be mounted in a single package. The development of bilateral or symmetrical PNP power transistors mounted three to a package (identical to the one containing the PNP Darlingtons) was also proposed. The triple PNP Darlington combination subsequently was given the designation L-173, and the triple symmetrical PNP's were given the number L-172. One L-173 and two L 172's were to be used per system.

In addition to these new transistor designs it was proposed that the two-chip, single package L-164 be used in three different locations in the regulator section of the inverter. Also, three NPN medium-power transistor drivers would be mounted in a single package. Several of these would be used in each inverter. This combination subsequently has been given the designation L-175.

Other special devices to be used were already scheduled for development under the original 75-VA contract. These included the single-chip divide-by-10 (L-168), divide-by-12 (L-167), divide-by-256 (L-166), and Johnson counter array (L-165).

The contract based on this proposal was awarded in May 1966 as a modification to the 75-VA contract.

Work began on the 100-VA on a limited basis in July 1966 with most of the available effort directed toward the 75-VA inverters. Low yields in the special power transistors (L-163 and L-164) being developed for the 75-VA inverters and extensive problems in the attempted development of the single-chip Johnson counter caused delays and unexpected expenses.

As a result, after the three 75-VA inverters had been delivered in March, 1967, it became obvious that additional funds would be necessary to complete the 100-VA portion of the contract. A further complication was concern about the technical feasibility of the development of the "triple" PNP power devices based on the experience gained in development of the 75-VA dual-chip power devices.

Consequently, in May a "Request For a Change in 100-VA Inverter Goals" (suggesting the substitution of the L-164 dual-power devices for the proposed triple-power devices) was submitted to NASA together with an estimate of the additional funds required. As an alternate approach, TI suggested later in May that two prototype inverters be developed using standard power transistors and that TI and NASA share the estimated cost on a 50/50 basis. NASA had no additional funds available to continue the program under either plan. Thus, this final report reviews progress on the 100-VA direct-coupled inverter program as of July 1, 1967.

SECTION II

PROGRESS ON SPECIAL SEMICONDUCTORS

A. L-172 AND L-173 DEVICES

The target specifications for the 100-VA power transistors were set as follows:

L-173 PNP Darlington

$$h_{FE}(\text{at } I_C = 5A,\ V_{CE} = -1.5\ V,\ T_A = 25°\,C) \geq 2000$$

$$BV_{CEO}(sus) \geq -60\ V$$

L-172 Symmetrical PNP

$$\text{Forward } h_{FE}(\text{at } I_C = -3A,\ V_{CE} = -1.0\ V,\ T_A = 25°\,C) \geq 30$$

$$\text{Inverse } h_{FE}(\text{at } I_C = -3A,\ V_{CE} = -1.0\ V,\ T_A = 25°\,C) \geq 15$$

$$BV_{CEO}(sus) \geq -60\ V$$

$$BV_{ECO}(sus) \geq -20\ V$$

Figures 17, 18, 19, 20 and 21 in the appendix are reduced photostatic copies of the drafting drawings for the PNP Darlington diffusion masks. The planar epitaxial device is made by diffusing impurities into a P-type silicon slice with a 1-mil, 6 to 10 Ω-cm epitaxial layer. Figures 22, 23, 24, 25, and 26 in the appendix are reduced photostatic copies of drafting drawings showing the diffusion mask design for the

symmetrical PNP. The large emitter area is necessary to keep the emitter and collector areas approximately equal, making the forward and inverse gain more nearly equal. The base is formed by epitaxially growing a 0.5-mil layer of 2 Ω-cm N-type silicon on a low-resistivity P-type substrate. The base contact and emitter are then diffused into the epitaxial layer. A P-type isolation diffusion through the epitaxial layer is necessary to make a planar collector-base junction.

The masks for both devices are available and some material was purchased. However, no devices have been diffused.

A significant amount of effort was expended in package design for the L-172 and the L-173. Reduced photostatic copies of the engineering drawings of the various package concepts are shown in the appendix, Figures 27 through 42.

B. L-163A AND L-164A DEVICES

The L-163A and L-164A dual-chip power transistors are the same devices as the L-163 and L-164 developed under the 75-VA contract with the exception of slightly different parameter specifications. The specification changes were initiated to make the devices compatible with both 75-VA-B and 100-VA usage. These devices are now being produced for the 75-VA-B inverter contract. The specification sheets for both devices are shown in Tables I and II.

C. L-175 DEVICE

The L-175 is a single package of three NPN medium power drivers. The package selected was the 16-pin industrial package used for the IC arrays (Figures 43, 44, and 45 in the Appendix). The transistor wafer used was from the 2N4001 family. The tentative specifications for this device are shown in Table III.

The first run of devices (approximately 75) were just fabricated and ready for electrical evaluation when work was curtailed. There is every indication that the yield of the devices to the tentative specification sheet would have been satisfactory.

D. L-166, L-167, and L-168 DEVICES

The divide-by-256 ripple counter (L-166), the divide-by-12 counter (L-167), and the divide-by-10 counter (L-168) IC arrays are identical to those used in the 75-VA inverter. These arrays had been fabricated and evaluated electrically and mechanically.

Table I. Electrical Specifications for L-163A *

Parameter		Test Condition	Min.	Max.	Unit
$V(BR)_{CEO}$	Collector-Emitter Breakdown Voltage	I_C = 30 mA, I_B = 0 (See Note 5)	75		V
I_{CEO}	Collector-Cutoff Current	V_{CE} = 50 V, I_B = 0 (See Note 5)		200	μA
I_{CES}	Collector-Cutoff Current	V_{CE} = 60 V, V_{BE} = 0			
		T_C = 150° C		5	mA
V_{BE}	Base-Emitter Voltage	I_B = 3.5 mA, I_C = 2.5 A (See Note 5)		2.1	V
$V_{CE\ (sat)}$	Collector-Emitter Saturation Voltage	I_B = 3.5 mA, I_C = 2.5 A (See Note 5)			
		T_C = −25° C		2.0	V
V_{EC_f}	Commutating-Diode Forward Voltage	I_C = −2.5 A, I_B = 0		1.3	V
	Secondary Breakdown	See Note 1			
	Power Dissipation Capability	See Note 2			
	Case Isolation	60 V applied between transistor case and any of six output pins. (See Note 4). Max. leakage current shall be 100 μA.			

Note 1. Test should be performed on the RCA secondary breakdown test set. No secondary breakdown should occur under the following conditions:

I_C = 10 A

L = 880 mH

5 ms, 10 pps, drive signal

No reverse bias voltage

I_B Forward = whatever is necessary to insure saturation at 10 amperes I_C.

The base resistance during the OFF interval should be 100Ω.

Note 2. An operating test shall be performed to determine the power dissipation capability of the device. The device shall be capable of dissipating six watts (10 V and 0.6 A) at ambient temperature of +125° C for 20 hours without drawing excessive current due to thermal runaway. A possible test circuit is shown in Figure 1.

Note 3. All data taken at +25° C unless otherwise noted.

Note 4. Should be tested after plating.

Note 5. These parameters must be measured using pulse techniques. T_p = 300 μs duty cycle ≤ 2%.

* Power Department Designation Number is SP4435

Table II. Electrical Specifications for L-164A *

Parameter		Test Condition	Min.	Max.	Unit
NPN-PNP	$V_{(BR)\ CEO}$	$I_C = -30$ mA, $I_B = 0$ (See Note 4)	100		V
NPN-PNP	$V_{CE(sat)}$	$I_C = -10$ A, $I_B = -10$ mA, $T_C = -25°$ C		-1.5	V
NPN-PNP	h_{FE}	$I_C = -10$ A, $V_{CE} = -2.5$ V (See Note 4)		8000	
NPN-PNP	I_{CES}	$V_{CE} = -60$V, $V_{BE} = 0$ $T_C = +150°$ C		10	mA
NPN	θ_{JC}			2	°C/W
PNP	BV_{EBO}	$I_E = 10$ mA	-5		V
NPN	Secondary Breakdown	See Note 1			
Case Isolation		60 V applied between transistor case and any of six output pins (See Note 3)		100	μA

Note 1. Forward secondary breakdown shall be tested by applying 20 V and 20 A simultaneously to the transistor for 12 ms at a duty cycle of 5 cpm.

Note 2. All readings at +25° C unless otherwise noted.

Note 3. Should be tested after plating.

Note 4. These parameters must be measured using pulse techniques. $T_p = 300\ \mu s$, duty cycle ≤ 2%.

Note 5. E, C, and B terminals will be as shown for NPN-PNP combination (See Figure 2)

* Power Department Designation Number is SP4436

Table III. Electrical Specifications for L-175 *

Triple NPN Medium Power Driver

Electrical characteristics at 25° C case temperature (unless otherwise noted)

Parameter		Test Conditions	Min.	Max.	Unit
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 30 mA, I_B = 0 (See Note 1)	100		V
I_{CEO}	Collector Cutoff Current	V_{CE} = 80 V, I_B = 0	30		μA
I_{CES}	Collector Cutoff Current	V_{CE} = 100 V, V_{BE} = 0, T_C = 150° C	150		μA
I_{EBO}	Emitter Cutoff Current	V_{ES} = 5, I_C = 0	1		μA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 0.5 V, I_C = 0.5 A, T_C = −25° C (See Note 5)	15		
V_{BE}	Base-Emitter Voltage	I_B = 20 mA, I_C = 0.5 A (See Note 1)		0.9	V
$\lvert h_{FE} \rvert$	Small Signal Common Emitter Forward Current Transfer Ratio	V_{CE} = 5 V, I_C = 0.5 A, f = 10 MHz	2		

Note 1. These parameters must be measured using pulse techniques.

T_P = 300 μs, duty cycle ≤ 2%.

Thermal Characteristics

Parameter		Max.	Unit
θ_{JC}	Junction-to-case Thermal Resistance of each transistor	50	°C/W
θ_{JA}	Junction-to-Free-Air Thermal Resistance of each transistor	250	°C/W

Absolute Maximum Rating:

Operating Collector Junction Temperature Range: −65°C to 200°C

* Power Department Designation Number is SP4437

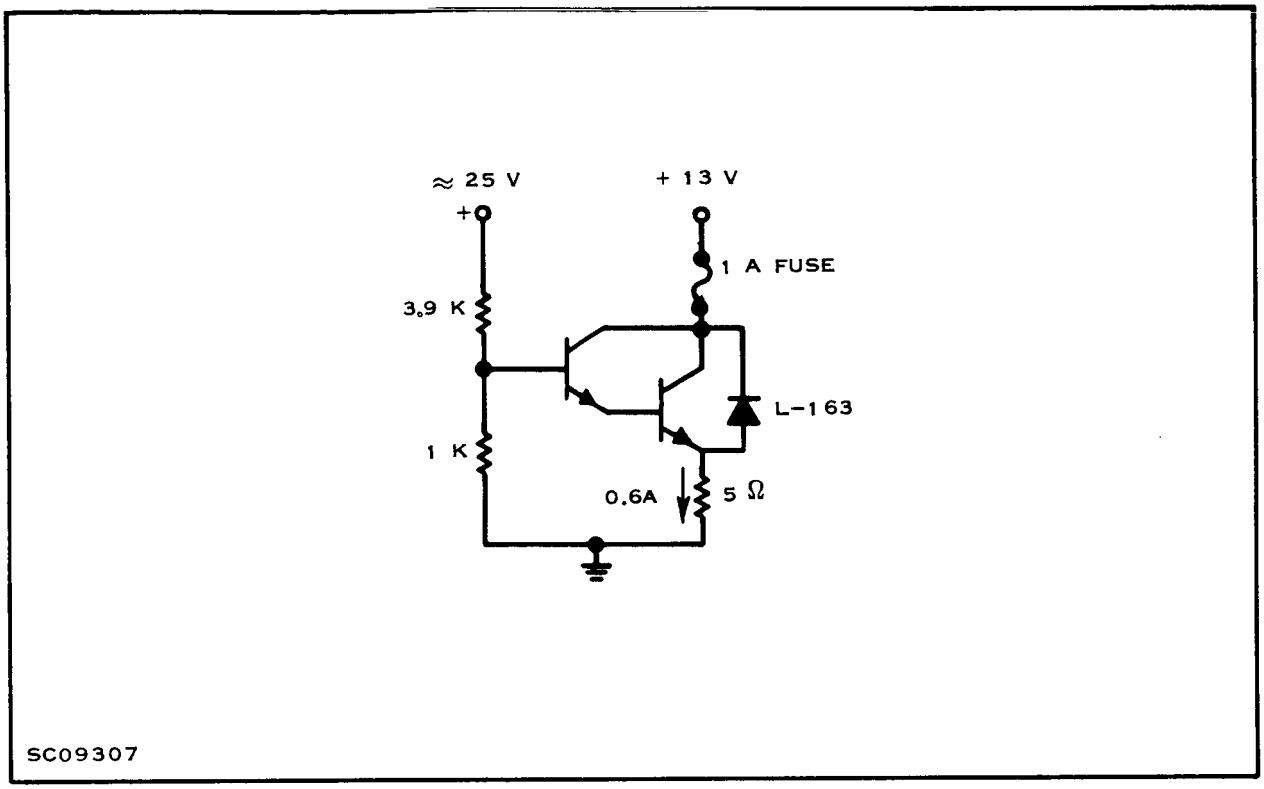


Figure 1. L-163 Test Configuration

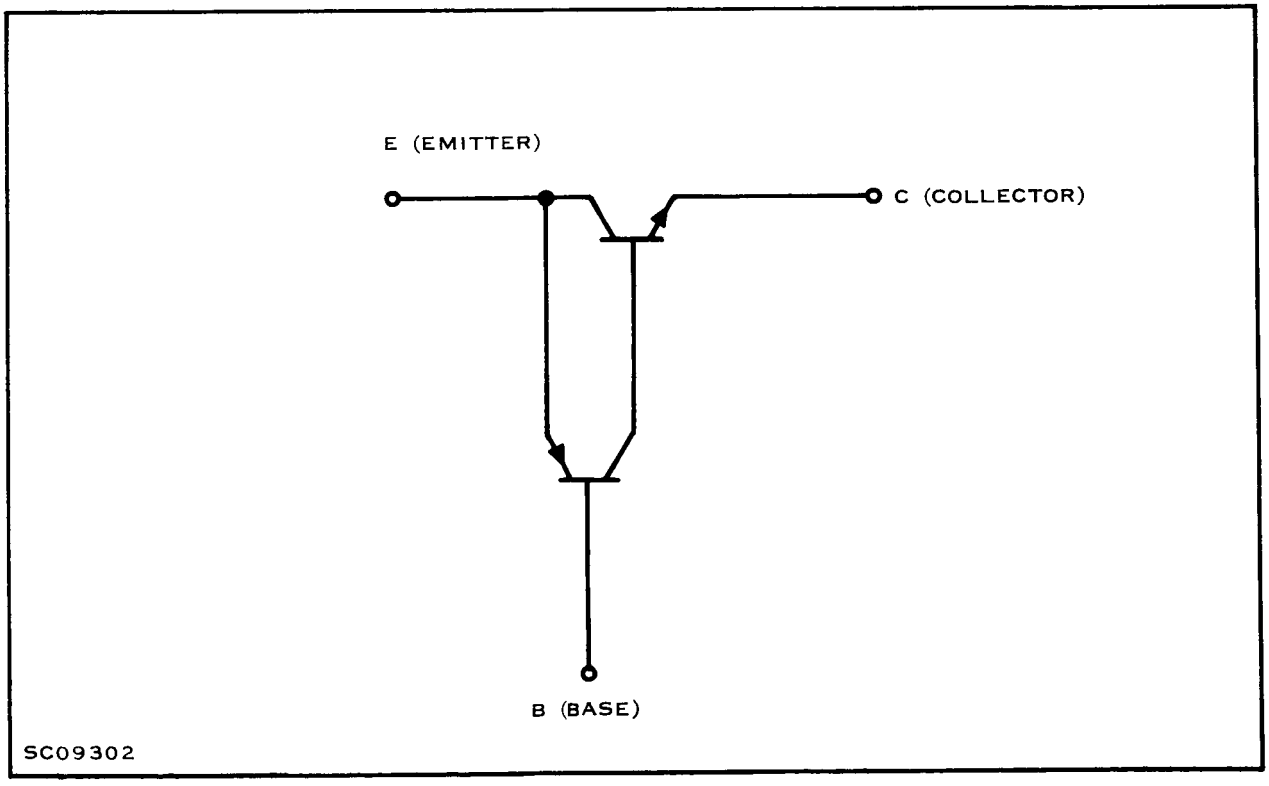


Figure 2. NPN-PNP Combination Configuration

SECTION III
CIRCUITRY

A. ACCOMPLISHMENTS

Circuit design of the 100-VA inverter (using standard power devices) is approximately 80 percent complete. A functioning breadboard was built; its block diagram and schematic are shown in Figures 3 and 4. The breadboard, although complete, still represents the estimated 80 percent complete status of the circuit design. Figure 5 contains a photograph of the breadboard which emphasizes the fact that bulky chokes, transformers, and capacitors are minimized in the direct-coupled approach. With the information presently available, it does not seem unreasonable to have a design goal for the 100-VA engineering model of 40 percent less size and volume than achieved with the 75-VA transformer-coupled inverter.

Final circuitry needs to be firmed up after an extensive evaluation of the breadboard performance under the various environmental and operational conditions. Also necessary is a careful comparison, under actual operating conditions, of the specified versus the actual ratings of the various components. These and other similar evaluations hopefully would reveal any circuit deficiencies that might exist. It would be expected that circuit modifications while certain and important would be minor in scope.

B. CIRCUIT IMPROVEMENTS

Although the 100-VA direct-coupled inverter shown in Figure 4 is basically the same circuit as the 75-VA direct-coupled inverter breadboard previously submitted to NASA, there are significant improvements. The inverter uses peak ac output current

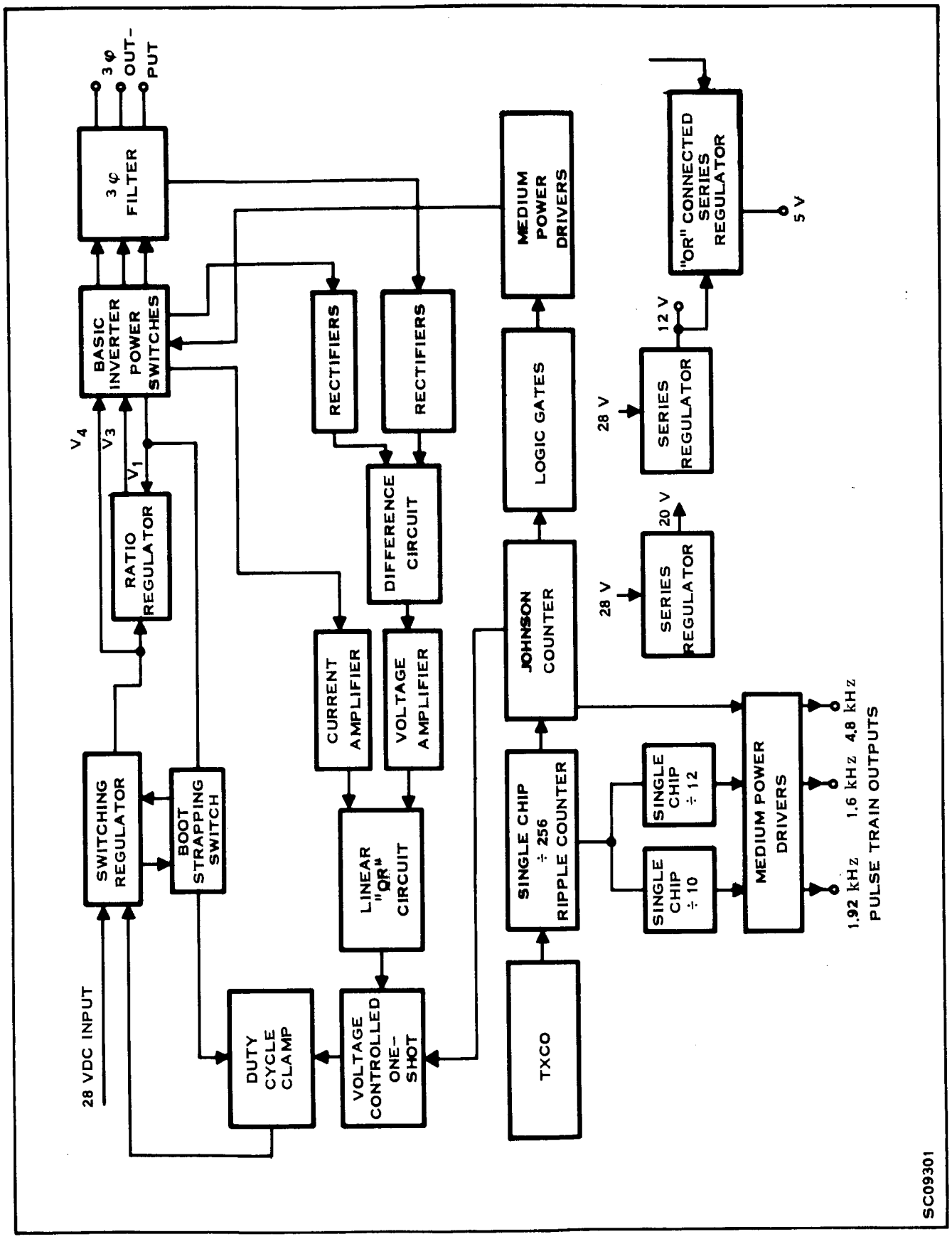
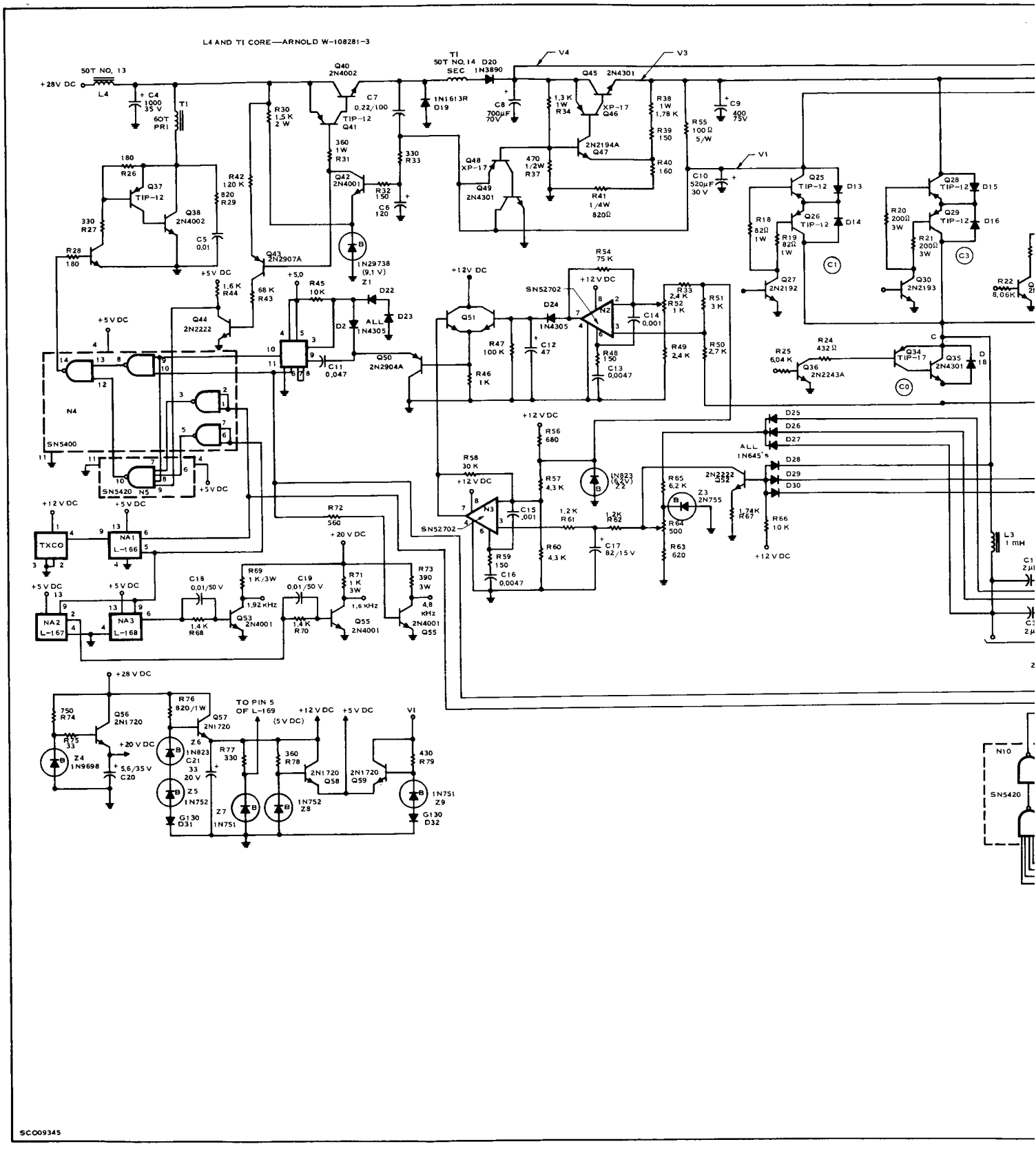


Figure 3. 100-VA Block Diagram


L4 AND T1 CORE—ARNOLD W-108281-3
+28V DC
50T NO. 13
L4
+ C4 1000 35 V
T1
60T PRI
Q40 2N4002
C7 0.22/100
TIP-12 Q41
T1 50T NO. 14 SEC
D20 1N3890
1N1613R D19
C8 700μF 70V
V4
V3
Q45 2N4301
XP-17 Q46
2N2194A Q47
Q48 XP-17
Q49 2N4301
R30 1.5K 2 W
R31 360 1W
R33 330
R32 150
C6 120
R34 1.3K 1W
R37 470 1/2W
R38 1W 1.78K
R39 150
R40 160
R41 1/4W 820Ω
R55 100Ω 5/W
C9 400 75V
C10 520μF 30 V
V1
Q25 TIP-12
D13
Q26 TIP-12
D14
R18 82Ω 1W
R19 82Ω 1W
Q27 2N2192
Q28 TIP-12
D15
Q29 TIP-12
D16
R20 200Ω 3W
R21 200Ω 3W
Q30 2N2193
C1
C3
R22 8.06K
R26 180
Q37 TIP-12
Q38 2N4002
C5 0.01
R27 330
R28 180
R42 120 K
R29 820
Q43 2N2907A
1N29738 (9.1 V) Z1
+5V DC
1.6 K R44
68 K R43
Q44 2N2222
+5,0
R45 10K
D22
D23
ALL 1N4305
D2
C11 0.047
Q50 2N2904A
+12V DC
Q51
R54 75 K
SN52702
D24 1N4305
C14 0.001
R33 2.4 K
R52 1 K
R51 3 K
R47 100 K
C12 47
R48 150
C13 0.0047
R49 2.4 K
R50 2.7 K
R46 1K
R24 432Ω
R25 6.04 K
Q36 2N2243A
Q34 TIP-17
Q35 2N4301
C0
N4
SN5400
SN5420 N5
R56 680
R58 30 K
R57 4.3 K
(1N823 (6.4V) Z2
D25
D26
D27
ALL 1N645's
D28
D29
D30
R65 6.2 K
Z3 2N755
2N2222 454
1.74K R67
R66 10 K
N3
C15 .001
1.2K R61
1.2K R62
R64 500
R63 620
R59 150
C16 0.0047
R60 4.3 K
C17 82/15 V
SN52702
R72 560
+20 V DC
TXCO
NA1 L-166
NA2 L-167
NA3 L-168
C18 0.01/50 V
C19 0.01/50 V
R69 1 K/3W
R71 1 K 3W
R73 390 3W
1.92 KHz
1.6 KHz
4.8 kHz
1.4 K R68
1.4 K R70
Q53 2N4001
Q55 2N4001
2N4001 Q55
L3 1 mH
N10
SN5420
+28 V DC
750 R74
Q56 2N1720
R75 33
Z4 1N9698
5.6/35 V C20
R76 820/1W
Q57 2N1720
Z6 1N823
C21 33 20 V
Z5 1N752
G130 D31
R77 330
Z7 1N751
TO PIN 5 OF L-169
(5 V DC)
360 R78
1N752 Z8
2N1720 Q58
2N1720 Q59
430 R79
1N751 Z9
G130 D32
VI

SC009345

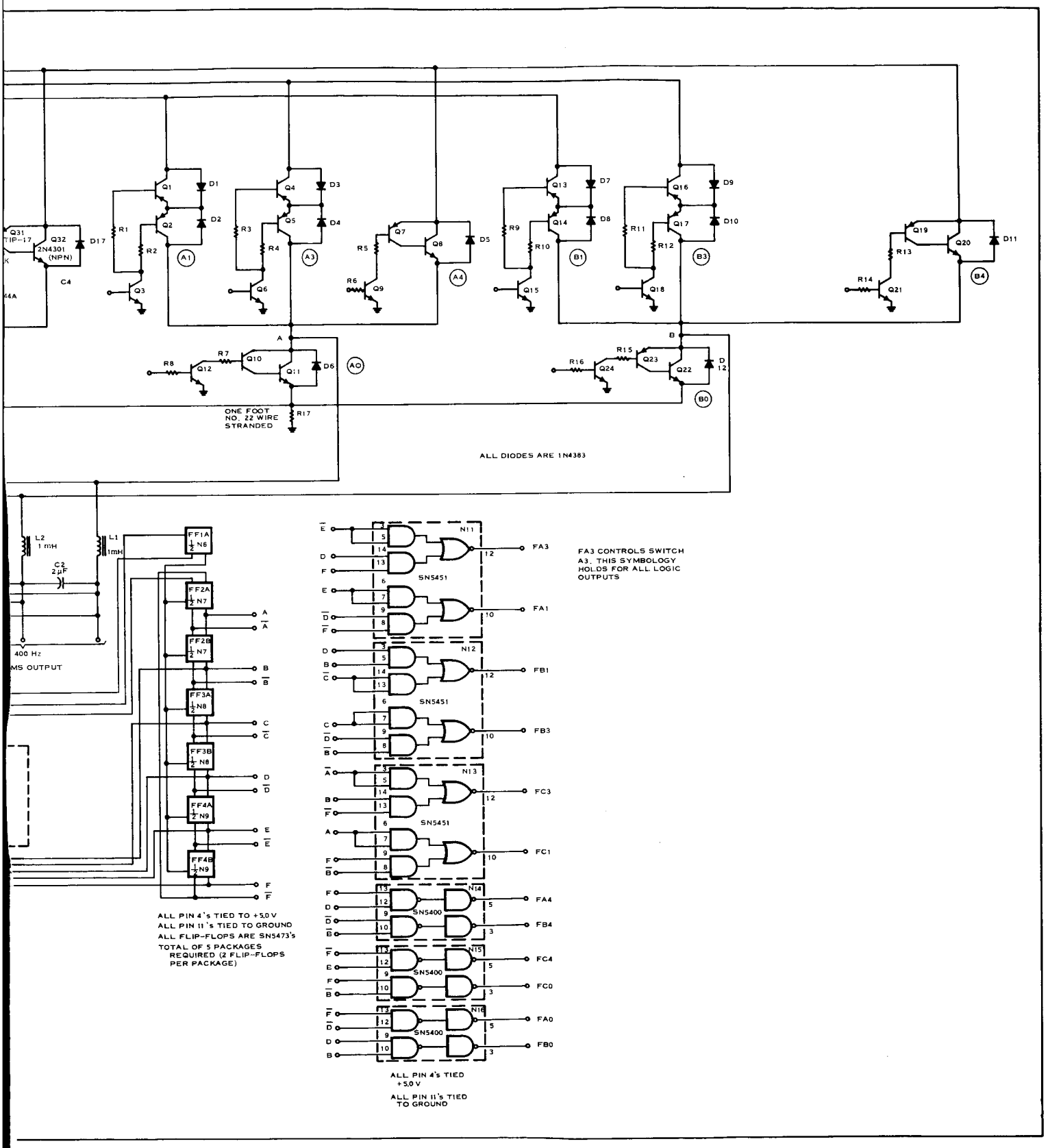


Figure 4. Preliminary Breadboard: 100 VA Direct-Coupled Static Inverter

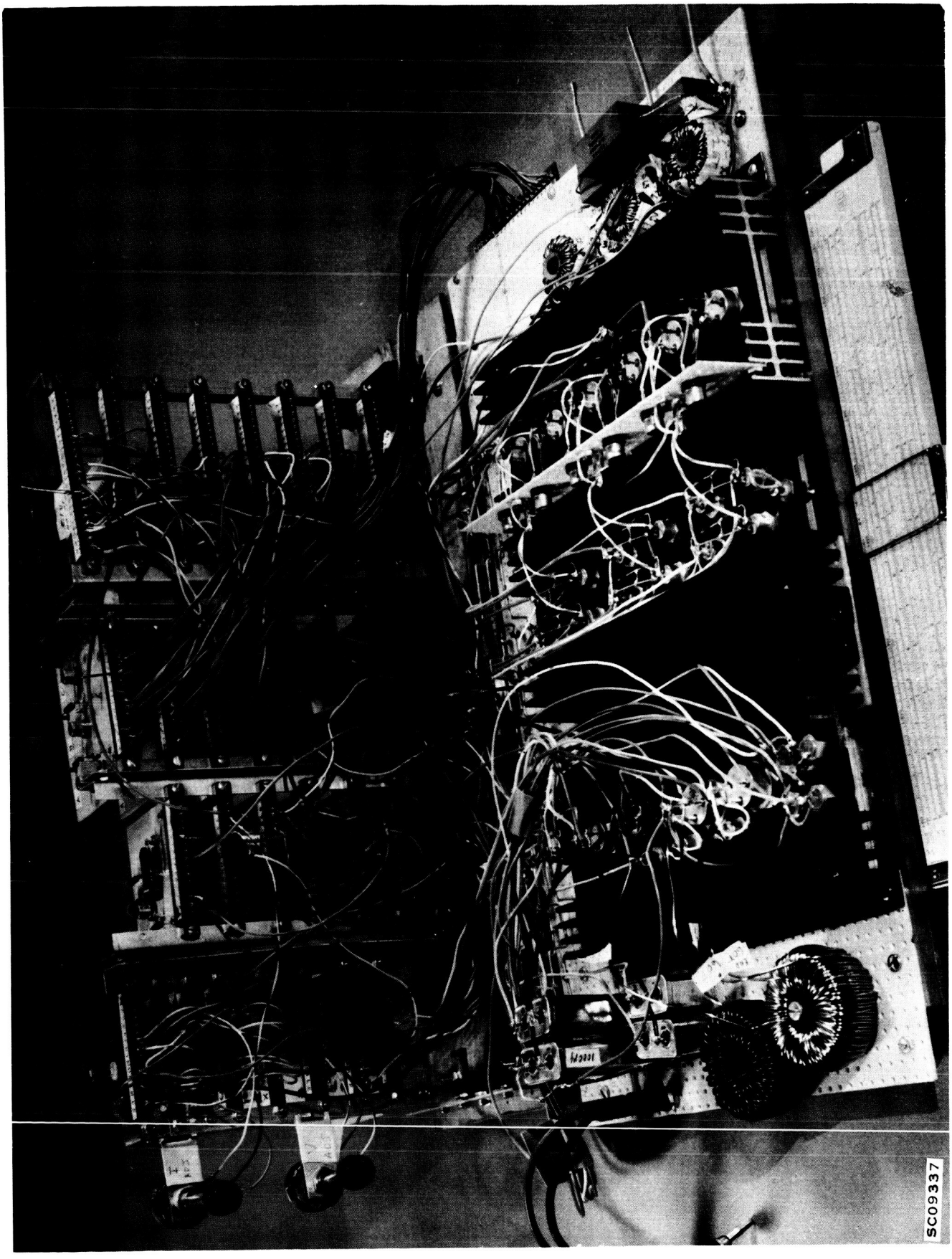


Figure 5. Direct-Coupled 100-VA Breadboard

limiting, which allows the inverter to handle unbalanced overloads. A duty cycle limiter circuit has been added to prevent excessive dc voltage from the switching regulator under certain transient conditions.

Better ac output waveshapes are obtained under light load and inductive loads with the synthesis of a truly symmetrical transistor by using two transistors and two diodes per switch.

The digital circuitry has been simplified and converted to Series 54.

The low-level linear circuitry has been improved to more readily utilize linear integrated circuits. Improved performance is believed to result from the use of a separate amplifier for the current and voltage sense circuitry.

The power devices selected represent a better selection in that they possess a greater safety margin of current and voltage capability.

C. CIRCUIT DETAILS

The unique feature of the direct-coupled inverter is the way it converts three levels of dc voltage to a three-phase ac voltage. For lack of a better name, that portion of the complete inverter which performs this function is called the "basic inverter." It is shown in simplified form in Figure 6.

A step-approximated sine wave appears between any two of the three nodes A, B, and C through the proper sequencing of the four switches connected to each node. The step-approximated shape (before filtering) will have approximately 15.2 percent total harmonic distortion and no harmonics below the 11th if the proper sequencing is used and if the three dc voltages V4, V3, and V1 are in the proper ratio. The proper ratios for V4, V3, and V1 respectively are 4:3:1.

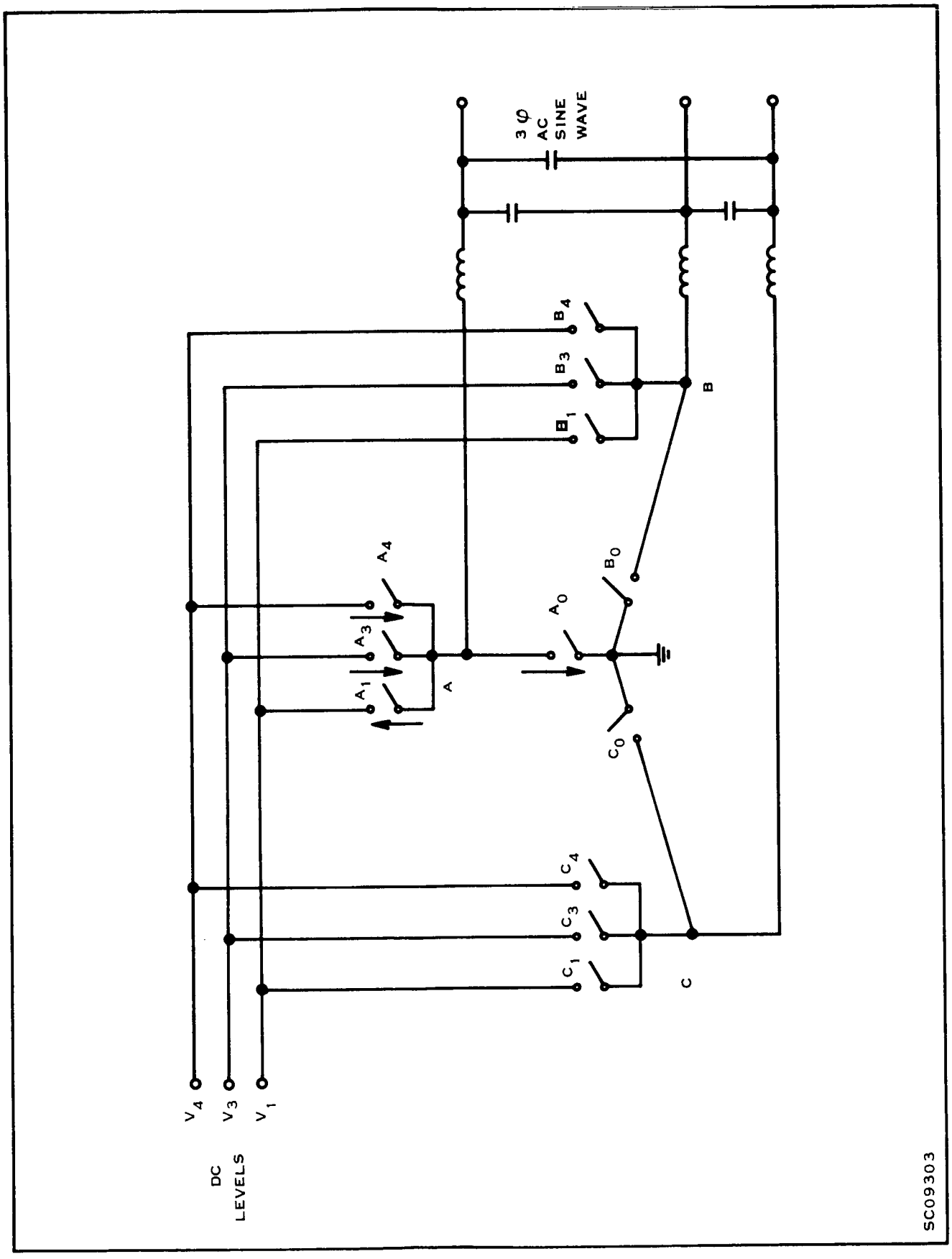


Figure 6. Basic Inverter and Three-Phase Filter

Current flows through each switch in the direction of the arrows shown by the "A" node switches. However, during light loads and inductive loads, the current direction will reverse for portions, or sometimes all, of the ON time of each switch. Therefore, to preserve the waveshape under such conditions, it is especially important for the "1" and "3" switches at each node to be capable of conducting in either direction. Figure 7 shows the configuration used to obtain the desired symmetrical switch characteristics.

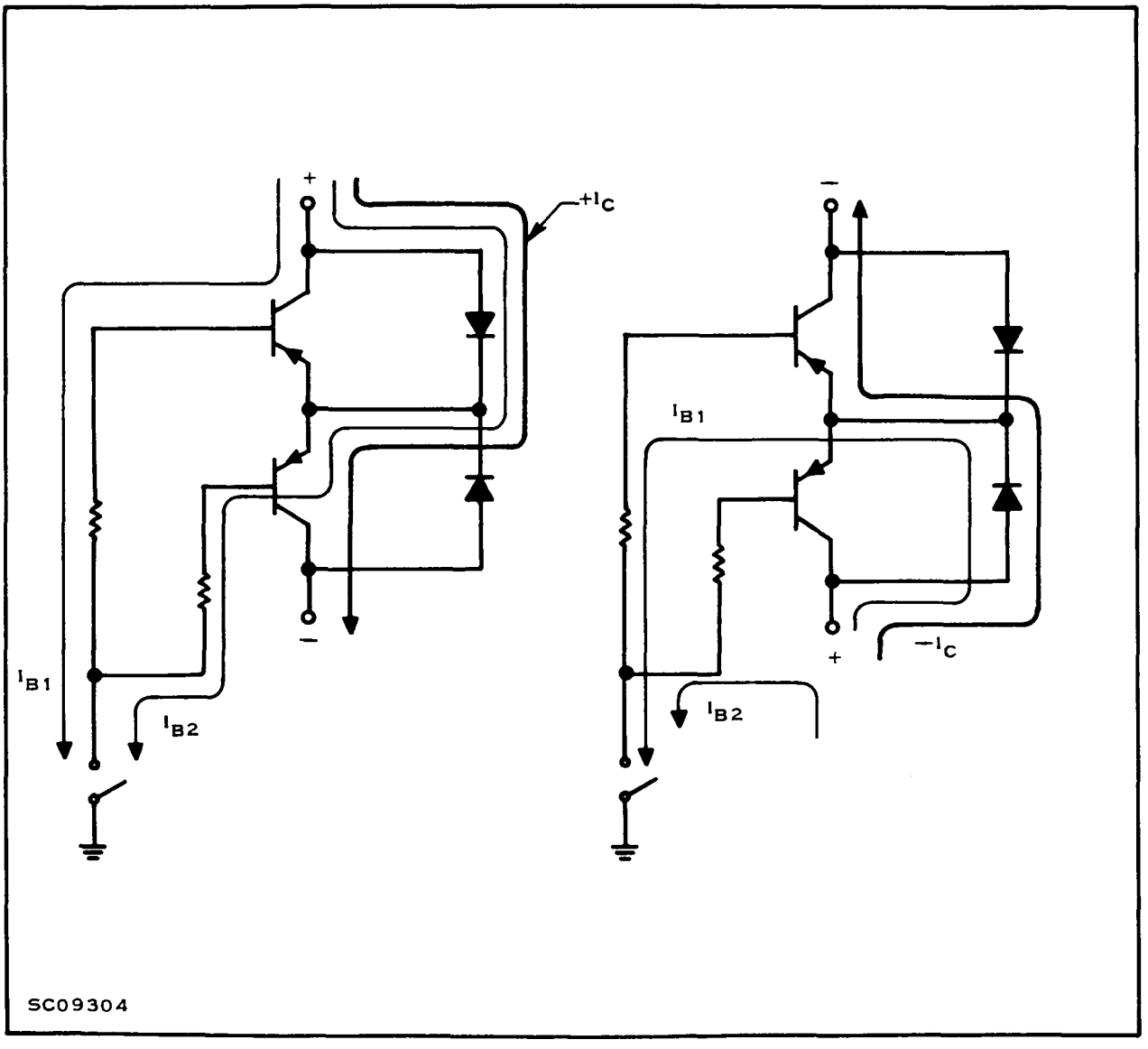


Figure 7. A Symmetrical Switch

Of the three dc voltage levels, V4 is obtained from a switching regulator. The voltage V4 also is the input to a linear regulator (Q45 through Q49 and associated circuitry in Figure 4) called the ratio regulator. The outputs of the ratio regulator are V3 and V1, both of which are always in the proper ratio of 3:1 with respect to V4 regardless of the magnitude of V4.

The peak value of ac output voltage is almost equal to V4. With the inverter operating in the constant voltage mode, V4 will necessarily be greater than the 28 volts dc input voltage. Conversely, V4 will be less than the dc input voltage under most overload conditions. A regulator that will fulfill these requirements and provide high efficiency under normal load is shown in elementary form in Figure 8. Under normal operation when a voltage step-up is required, Q40 is ON all the time and Q39 is duty-cycle modulated to provide the desired output. Energy is stored in transformer T1 by charging the

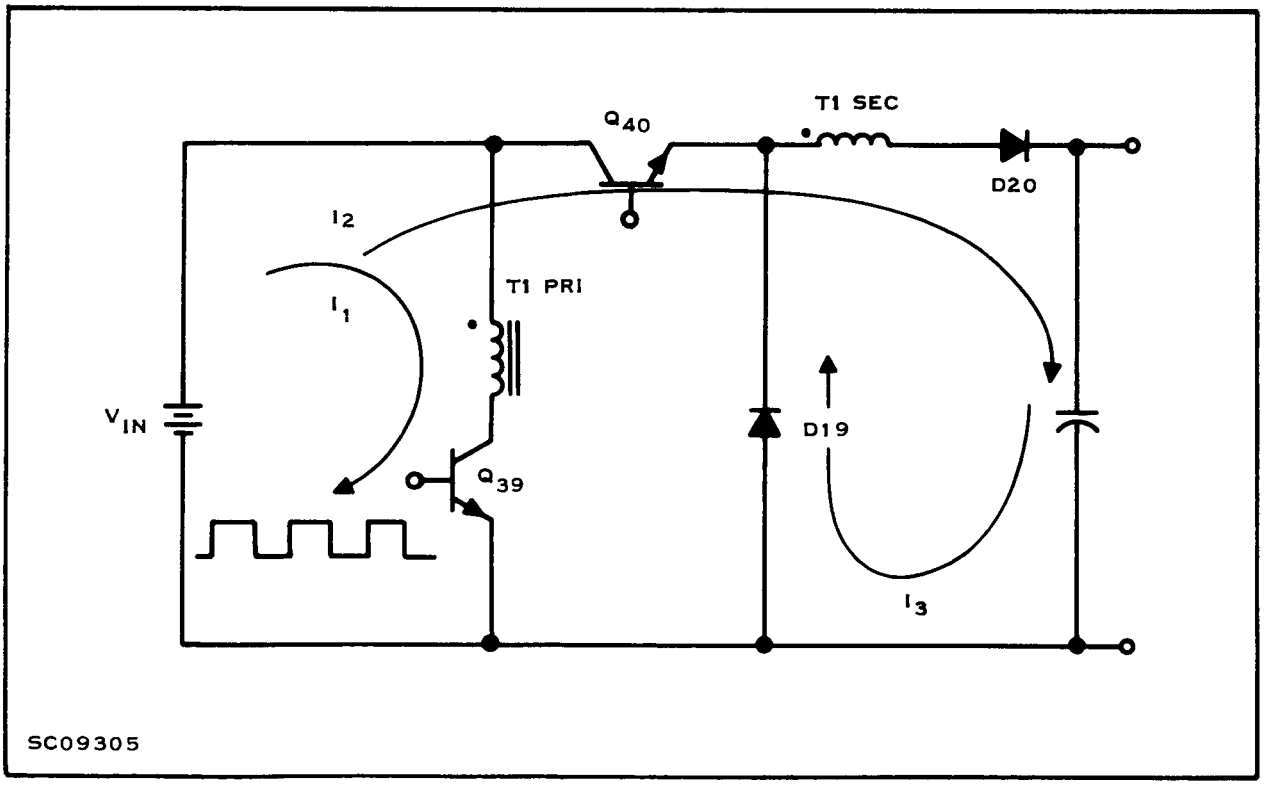


Figure 8. Switching Regulator

primary through loop I_1 and alternately discharging the secondary into the load (R and C) through loop I_2. Operating under this condition (known as bootstrapping) the regulator generates only the difference between the input and output voltages; hence, overall regulator efficiency is high. The output voltage, when in the bootstrapping mode, is given by

$$V4 \approx V_{in} + \frac{N_S}{N_P} \left(\frac{\tau}{1-\tau}\right) \quad (1)$$

When it is necessary to drop V4 below V_{in} (e.g., during overload), Q40 is turned OFF full-time and Q39 is duty-cycle modulated to give the desired output voltage. The primary of T1 is still charged by loop I_1, but is now discharged into the load through loop I_3. Thus, all the energy is transferred magnetically from V_{in} to V4. The efficiency is lower than it is in the bootstrapping mode, but it does allow V4 to drop to any level below V_{in}. The expression for output voltage without bootstrapping is

$$V4 \approx V_{in} \quad \frac{N_S}{N_P} \left(\frac{\tau}{1-\tau}\right) \quad (2)$$

where, both Equations (1) and (2), τ is the ratio of ON time to the period of the pulse train. As can be seen from Equations (1) and (2), a large value of duty cycle will result in a large value of V4.

The purpose of the N4 and N5 circuitry (see Figure 4) is to prevent an excessive value of V4 from occurring during transient conditions of initial turn-on or rapid change from a load to no-load condition. The logic enables the variable duty cycle pulse train obtained from N1 (variable duty cycle one-shot) to be passed unmodified only as long as: (1) the switching regulator is in the bootstrapping mode and has a duty cycle of 50 percent or less, or (2) the switching regulator is in the non-bootstrapping mode and has a duty cycle of 62.5 percent or less. Whenever any of these limits are exceeded by the N1 output, the N4 and N5 circuitry clamps the pulse train duty cycle at the maximum value appropriate to the mode of switching regulator operation at that time.

Another portion of Figure 4 which may need an explanation is the voltage difference circuit, shown separately in Figure 9. The purpose of the circuit is to obtain a dc voltage proportional to the value of ac output phase-to-phase voltage, which can be used as a control voltage to regulate the ac output. Diodes D25, D26, and D27 are diode OR circuits that provide an output of the peak value of ac output phase-to-ground voltage. This voltage is directly proportional to the phase-to-phase output voltage, except that it contains an additional component of voltage from the saturation voltage of the power switches A_0, B_0, and C_0.

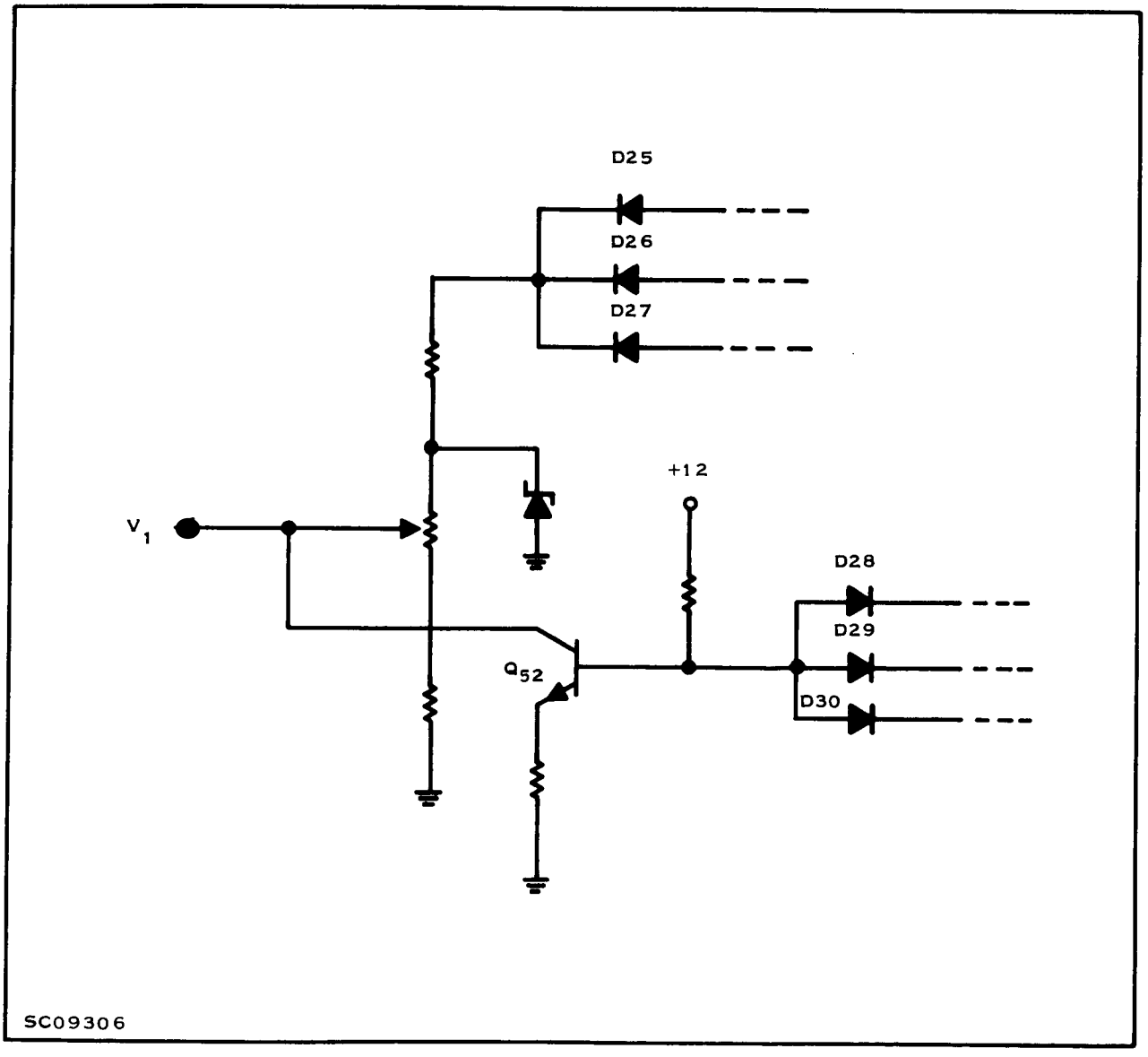


Figure 9. Voltage Difference Circuit

Diodes D28, D29, and D30, also diode OR circuits, have an output that is the saturation voltage of switches A_0, B_0, and C_0. The voltage V1 can be shown to be almost a direct function of the instantaneous difference between the two voltages. Consequently V1 is an almost direct function of the ac output phase-to-phase voltage as well.

D. BREADBOARD PERFORMANCE

Time did not permit a complete evaluation of the breadboard performance at room temperature—much less at the temperature extremes. However, the performance data available is presented here along with some photographs of interesting waveforms.

Figure 10 shows the output waveforms for various conditions of loading. Figure 11 shows typical worst-case repetitive current waveforms in the power switches (A_4, A_3, A_1) of the basic inverter. The current waveform for the A_0 switch is identical to that for A_4.

Figure 12 is the worst-case repetitive current and voltage waveform experienced by the main switching regulator transistor Q38 of Figure 2.

A typical phase-to-ground and phase-to-phase voltage waveform obtained from the basic inverter prior to filtering is shown in Figure 13.

The regulation of ac outputs is shown in Table IV.

Information concerning the inverter efficiency, ac output distortion, and ac output voltage,and current characteristic are shown in the curves of Figures 14, 15, and 16, respectively.

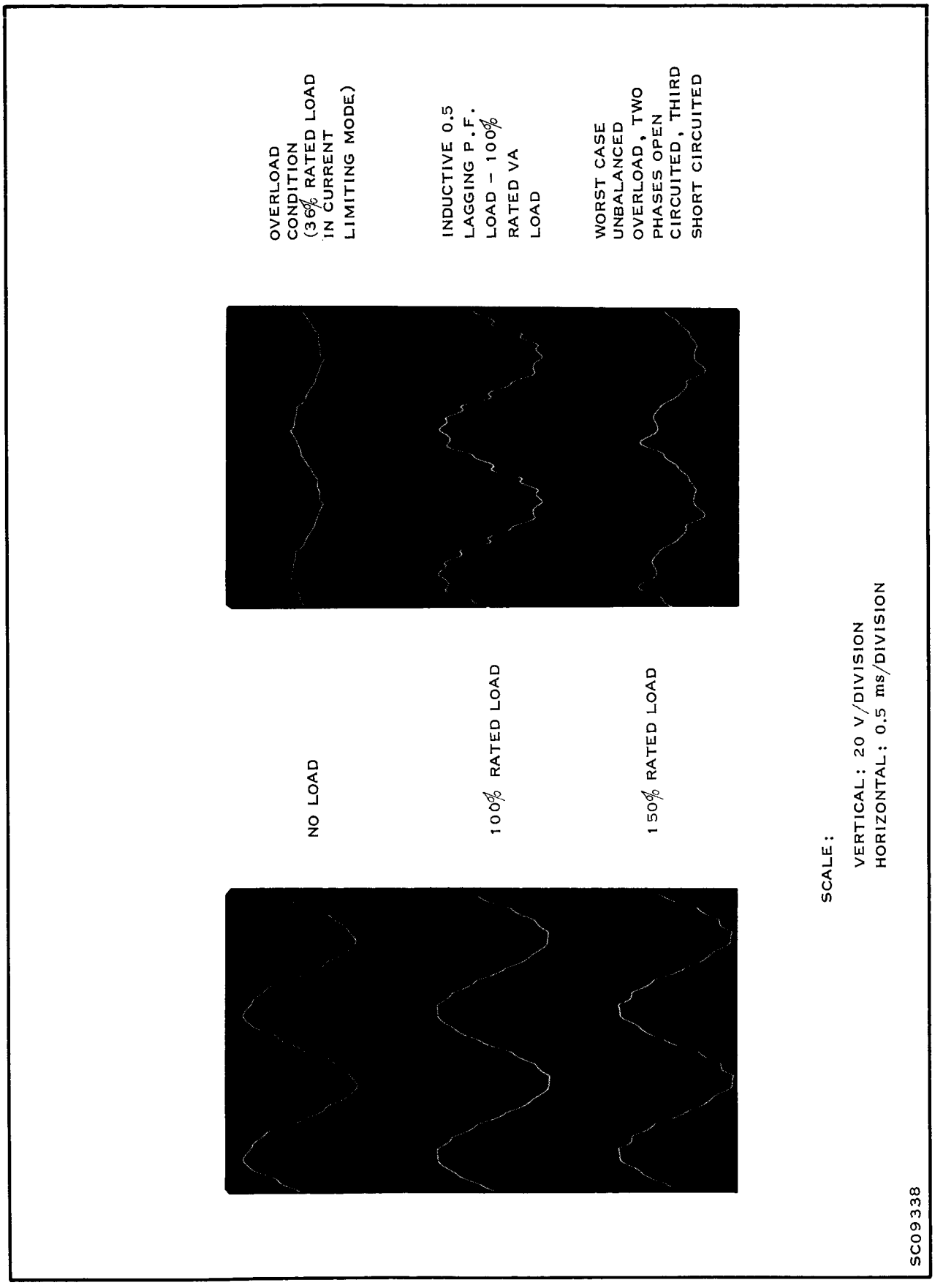


Figure 10. Output Waveforms

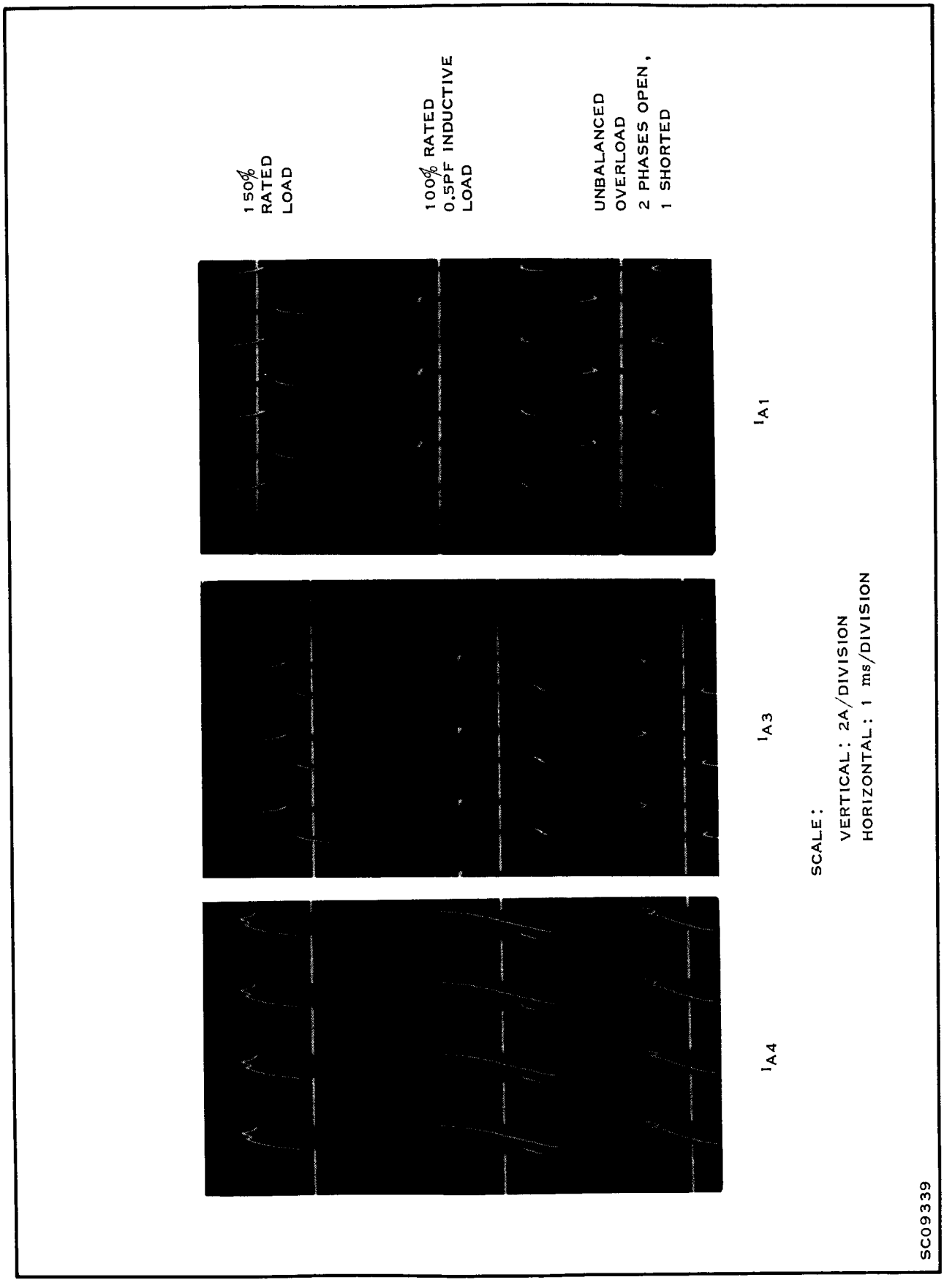


Figure 11. Typical Collector Currents in Switches of Basic Inverter

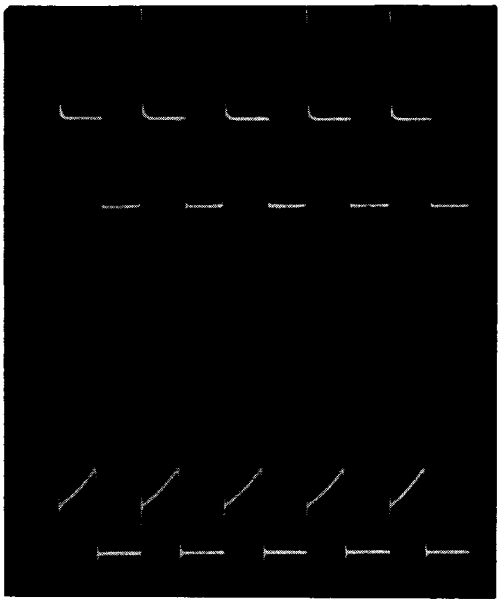


Figure 12. Q38 Current and Voltage Waveforms at 150% of Rated Load

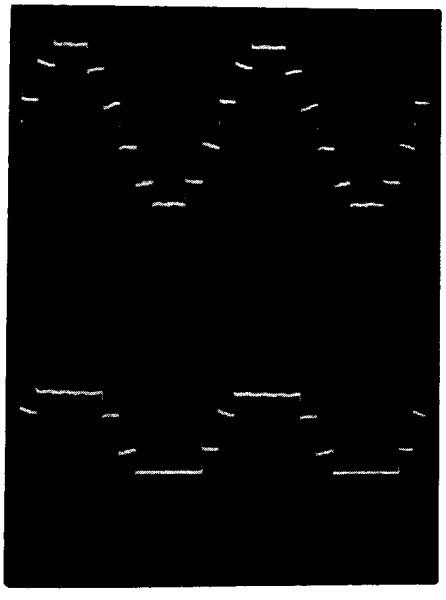


Figure 13. Basic Inverter Voltage Waveforms Before Filtering

Table IV. Inverter Regulation Data

% Rated P_o / V_{in}	Constant Voltage Mode			Current Limited Mode		
	$R_L = \infty\ \Omega$ 0%	$R_L = 205\Omega$ 10%	$R_L = 20\Omega$ 100%	$R_L = 13.4\Omega$ 150%	$R_L = 3.5\Omega$ 37%	$R_L = 0\Omega$ 0%
25VDC	V_{AB} 26.0 V_{BC} 25.9 V_{CA} 25.9	V_{AB} 26.4 V_{BC} 26.4 V_{CA} 26.4	V_{AB} 25.9 V_{BC} 25.9 V_{CA} 25.9	V_{AB} 25.3 V_{BC} 25.3 V_{CA} 25.3	V_{AB} 6.5 V_{BC} 6.5 V_{CA} 6.5	—
28VDC	V_{AB} 26.1 V_{BC} 26.0 V_{CA} 26.0	V_{AB} 26.5 V_{BC} 26.5 V_{CA} 26.5	V_{AB} 26.0 V_{BC} 26.0 V_{CA} 26.0	V_{AB} 26.0 V_{BC} 26.0 V_{CA} 26.0	V_{AB} 6.6 V_{BC} 6.6 V_{CA} 6.6	—
31VDC	V_{AB} 26.2 V_{BC} 26.1 V_{CA} 26.1	V_{AB} 26.6 V_{BC} 26.6 V_{CA} 26.6	V_{AB} 26.1 V_{BC} 26.1 V_{CA} 26.1	V_{AB} 26.0 V_{BC} 26.0 V_{CA} 26.0	V_{AB} 6.6 V_{BC} 6.7 V_{CA} 6.7	—

Note: R_L is the value of each resistor in a balanced three-phase delta load.

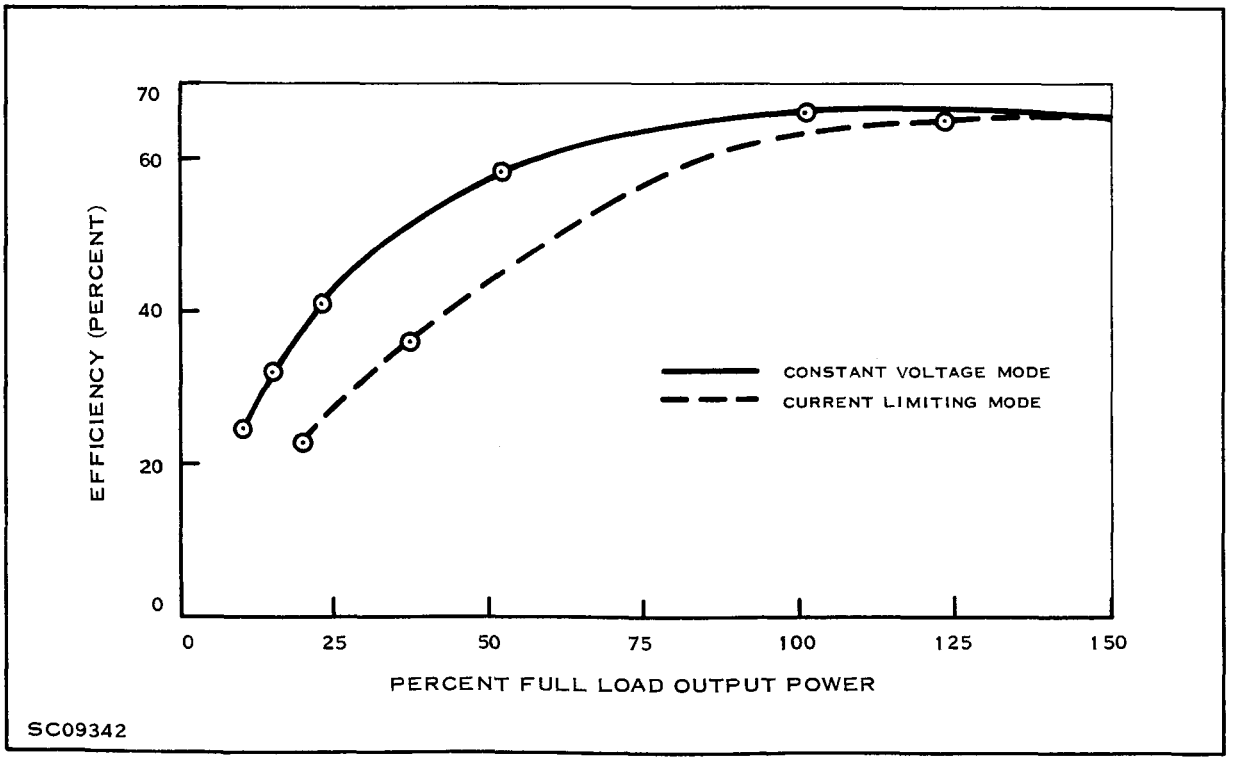


Figure 14. Inverter Efficiency

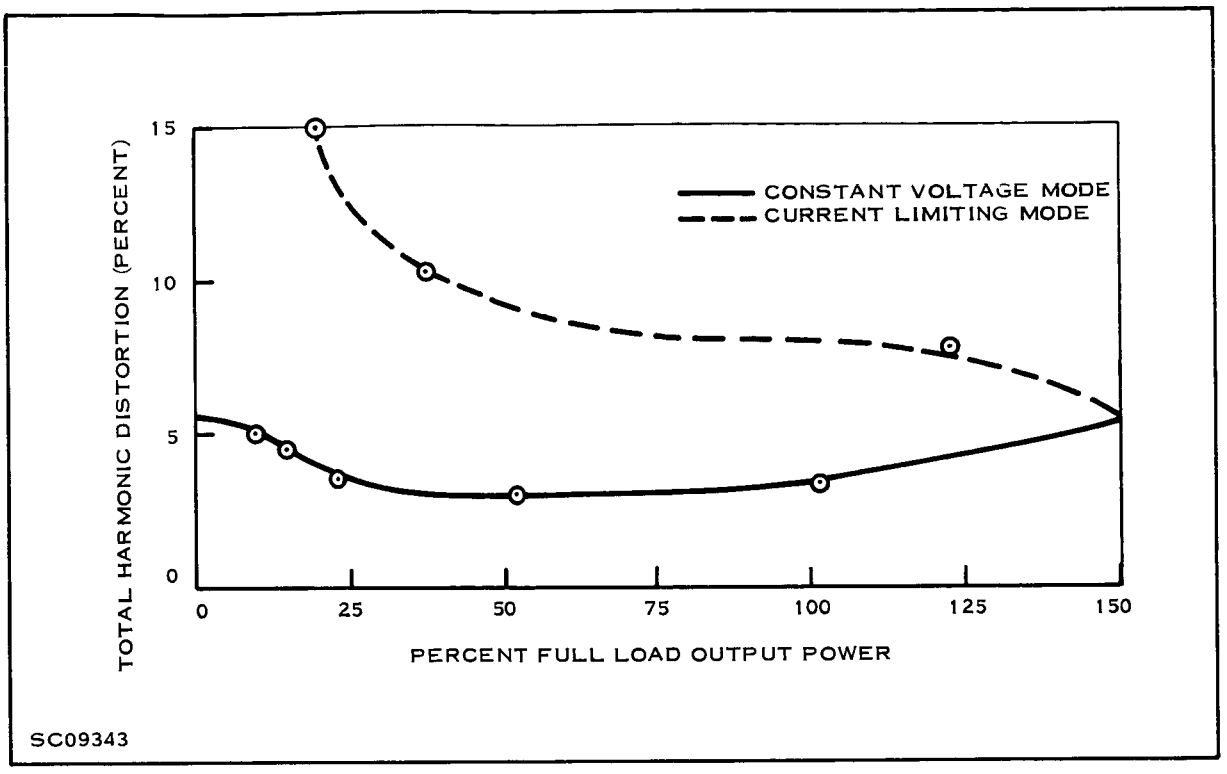


Figure 15. Distortion of Output Waveform

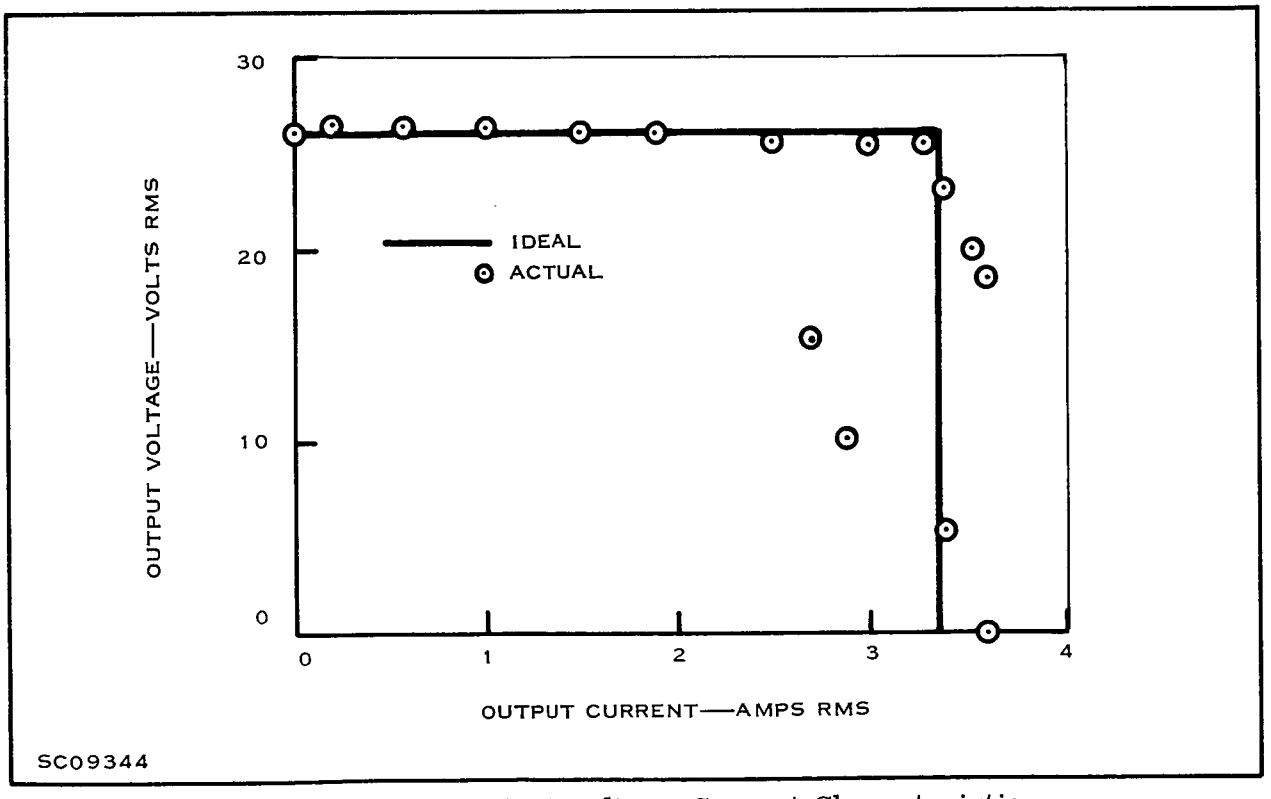


Figure 16. Output Voltage-Current Characteristic

SECTION IV

RECOMMENDATIONS

Early in the contract NASA officials asked for comments on the possibility of designing a direct-coupled inverter for a 12 V or 6 V ac output. At that time the special, triple-power transistors were considered a major problem, and the necessary additional current handling capability they would have required caused us to advise against such an approach.

As it turned out, however, the 100-VA direct-coupled inverter was designed with standard off-the-shelf power transistors. With standard transistors, there is no reason why a low output voltage direct-coupled inverter should not be readily attainable. It would even have one major advantage over the 26 V output inverters. A switching regulator with the capability of stepping up the dc voltage would not be necessary, thus resulting in a significant savings in circuitry.

APPENDIX

REDUCED PHOTOSTATIC COPIES OF DRAFTING DRAWINGS FOR THE 100-VA STATIC INVERTER

(Figures 17 through 45)

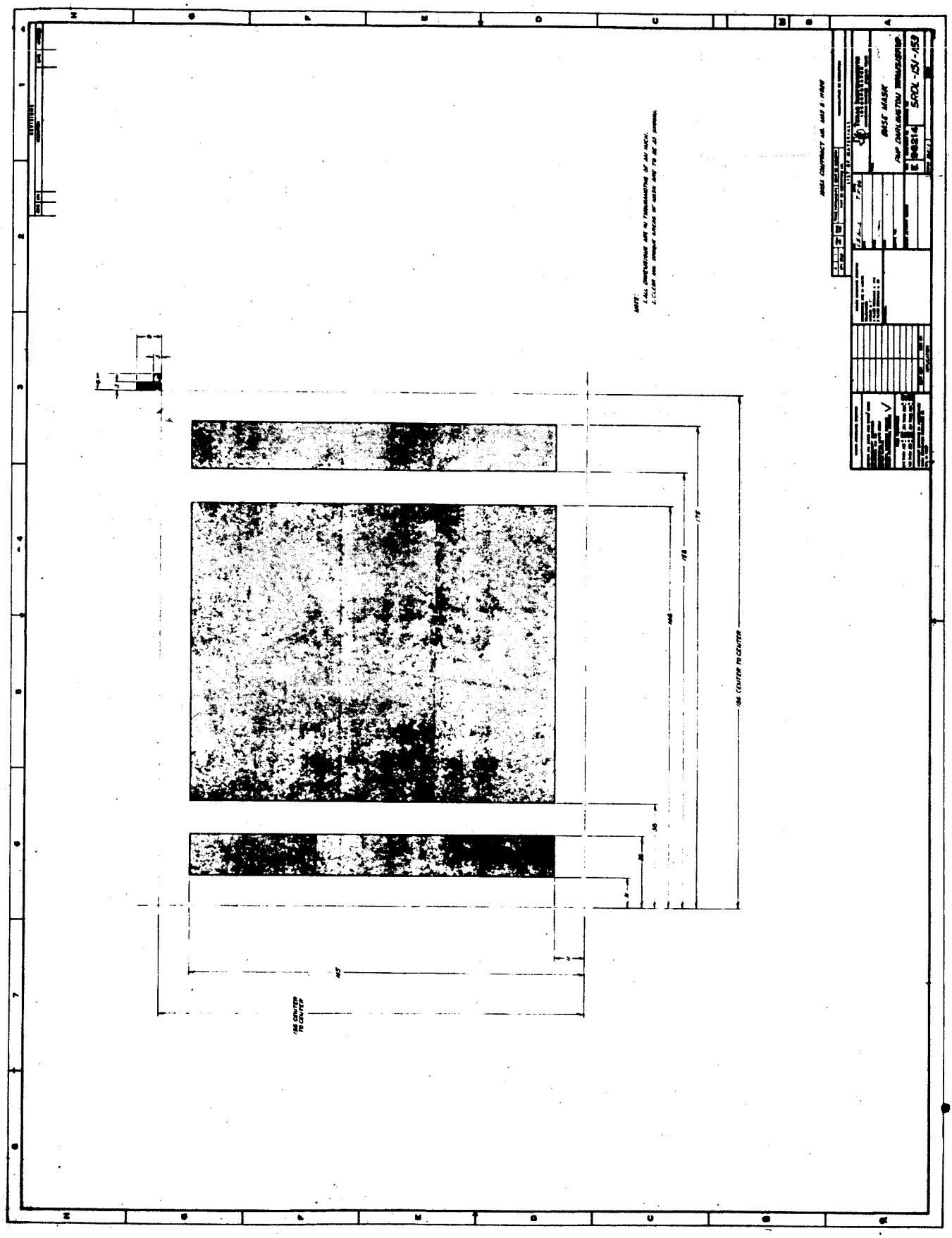


Figure 17. Base Mask, PNP Darlington Transistor

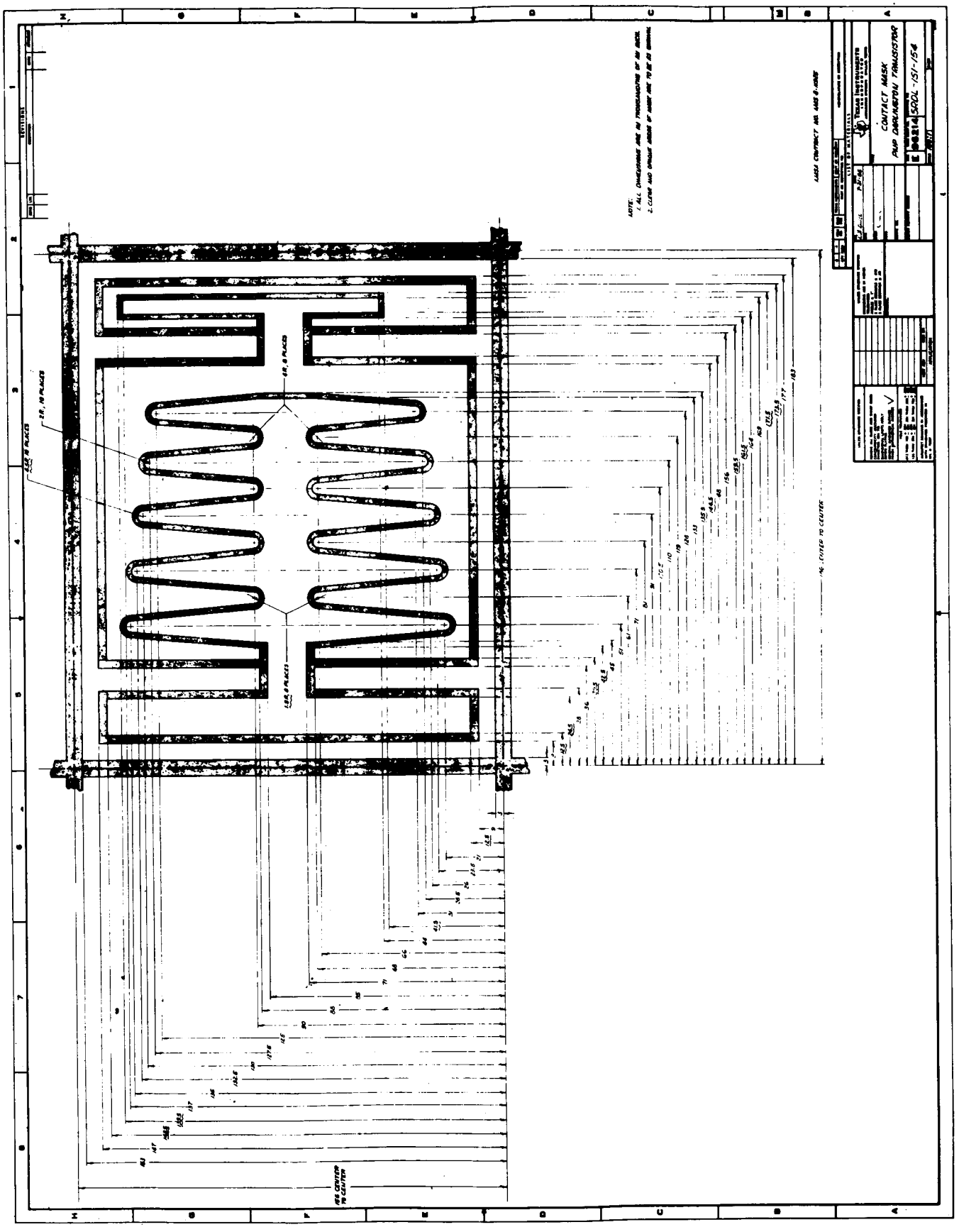


Figure 18. Contact Mask, PNP Darlington Transistor

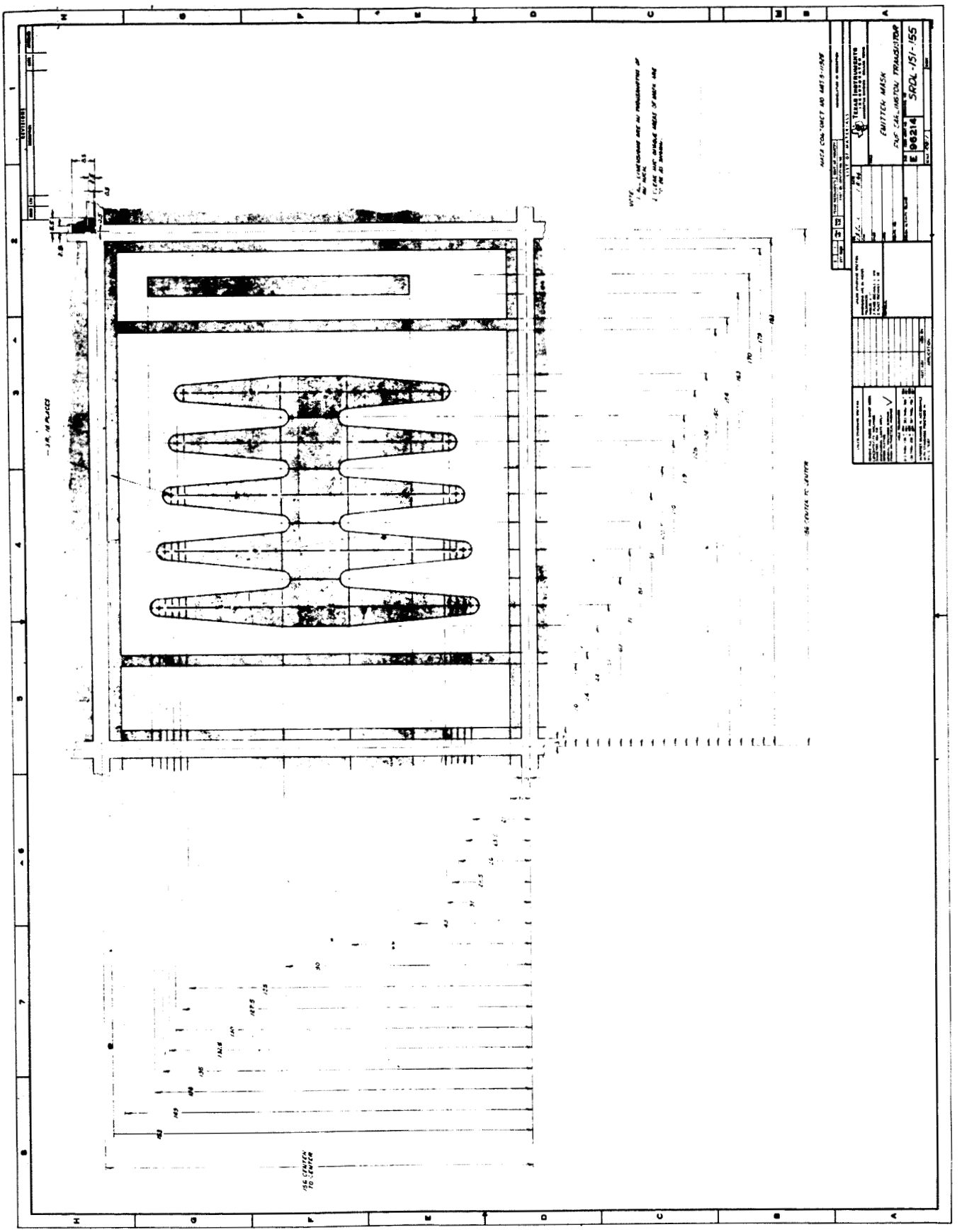


Figure 19. Emitter Mask, PNP Darlington Transistor

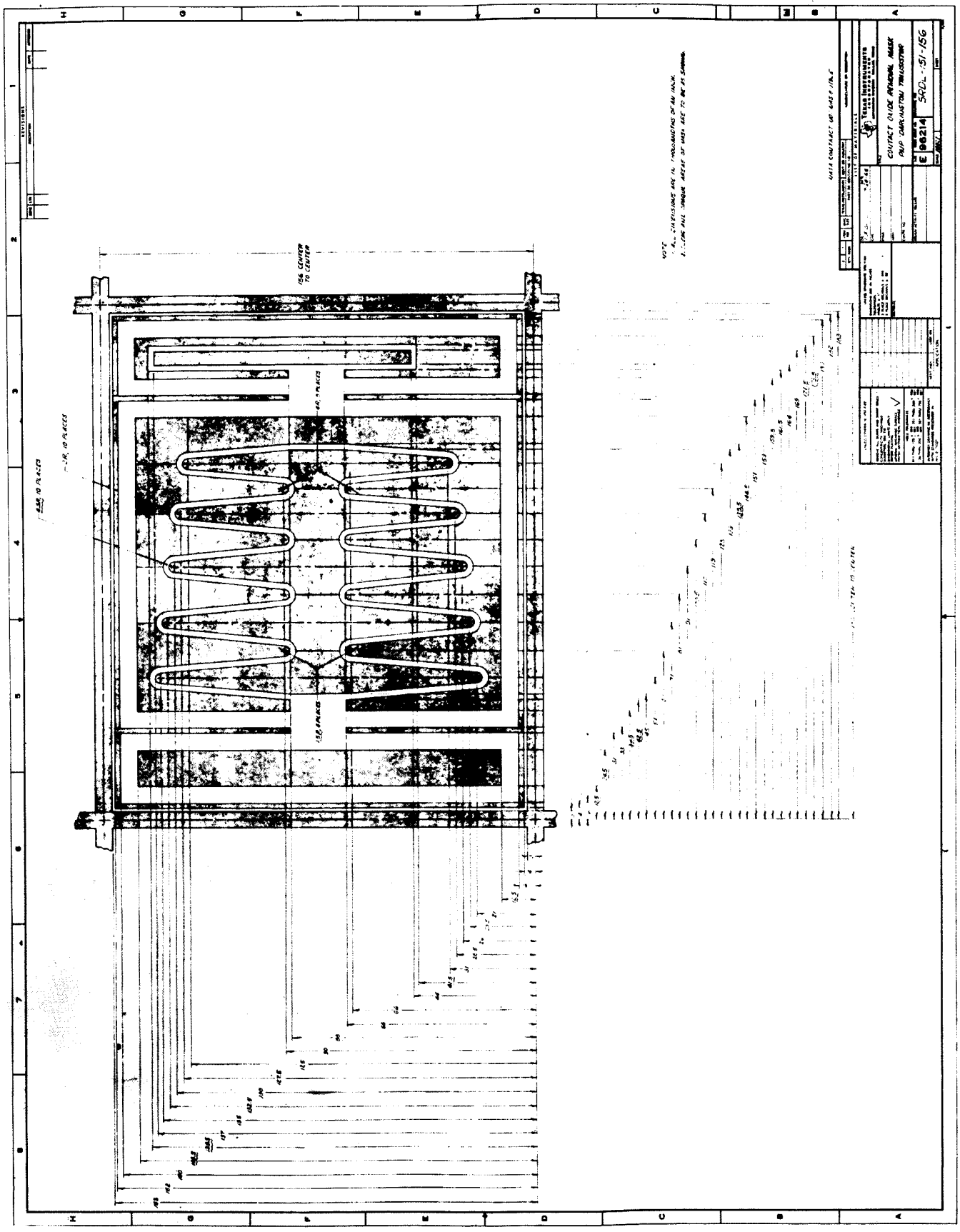


Figure 20. Contact Oxide Removal Mask, PNP Darlington Transistor

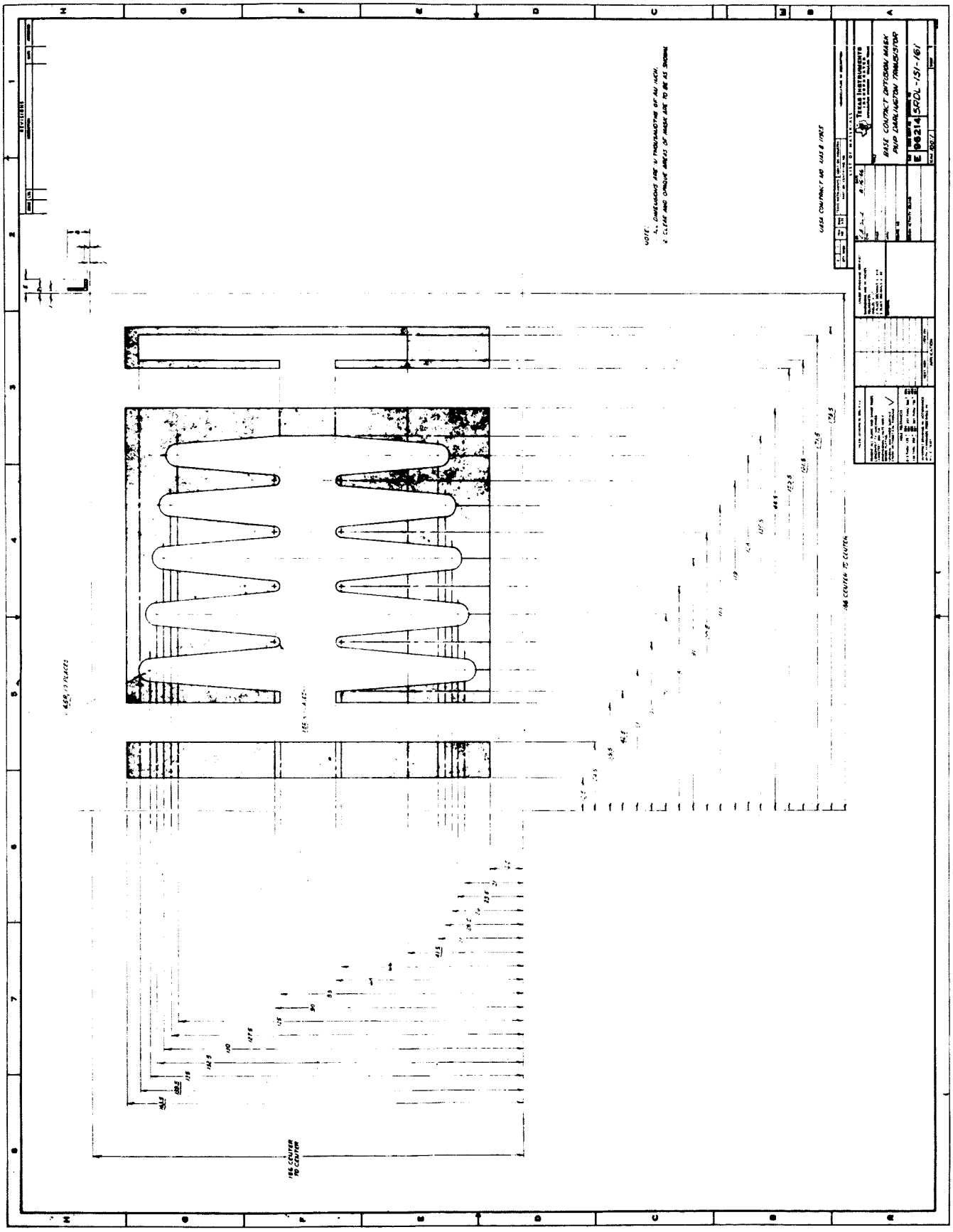


Figure 21. Base Contact Diffusion Mask, PNP Darlington Transistor

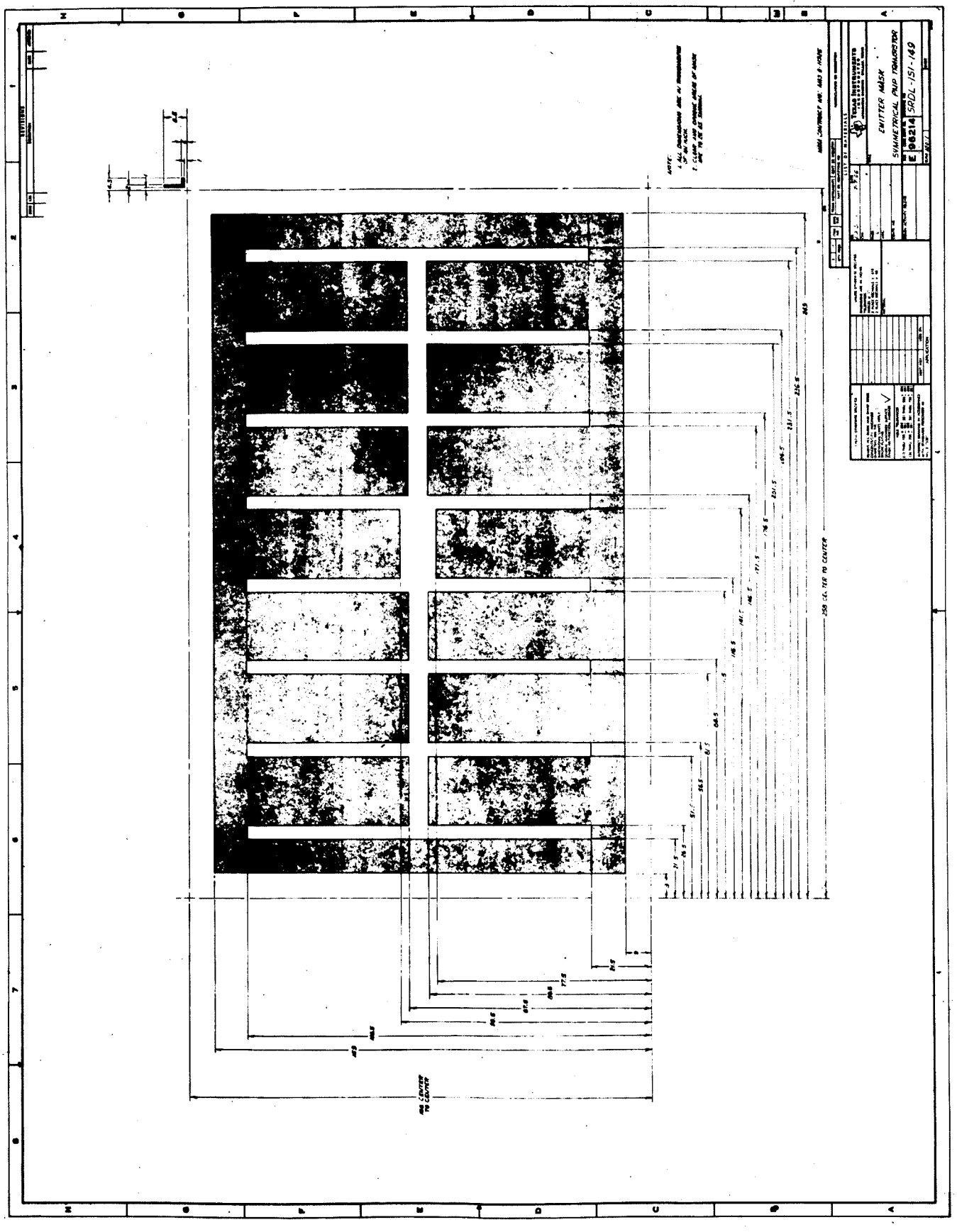


Figure 22. Emitter Mask, Symmetrical PNP Transistor

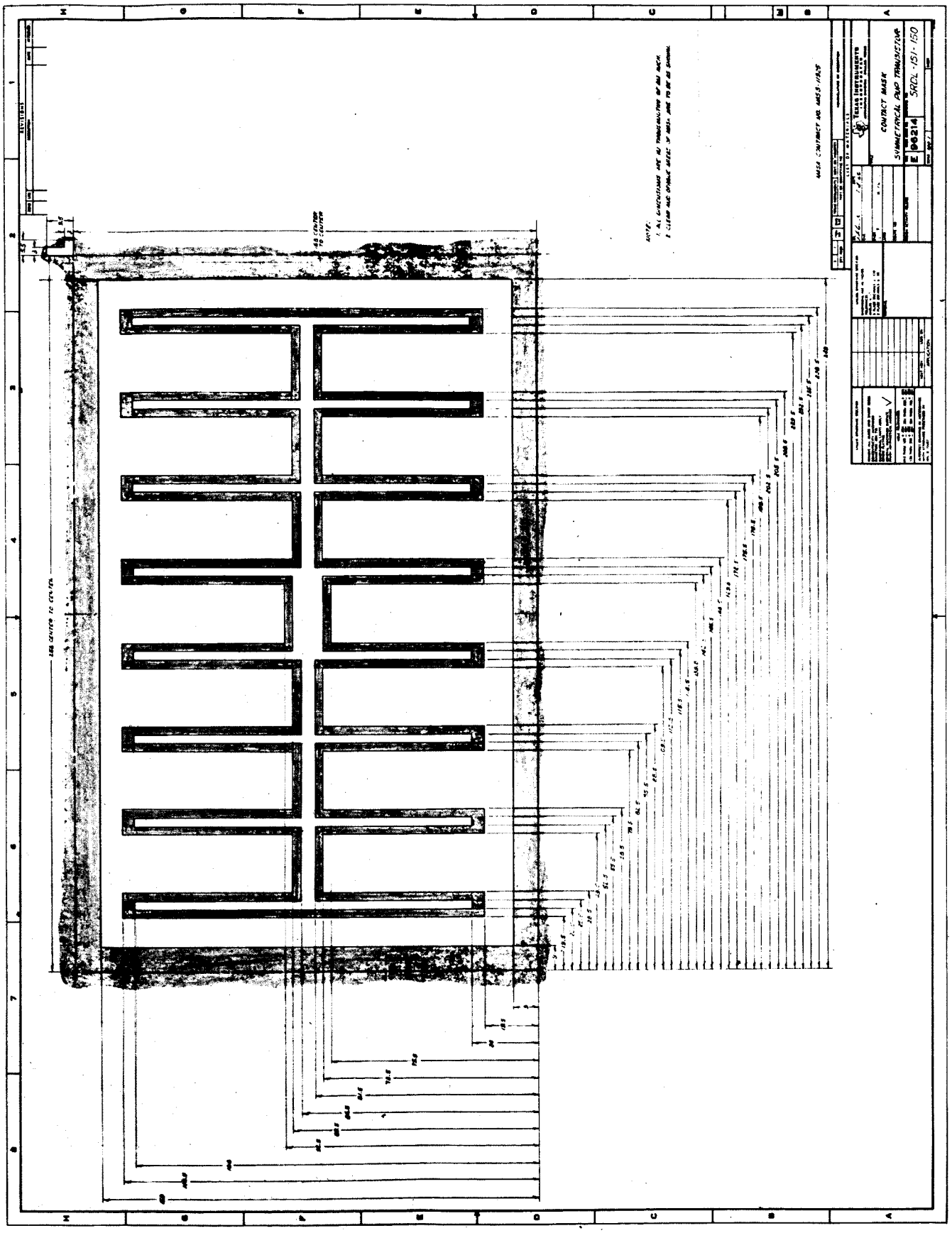


Figure 23. Contact Mask, Symmetrical PNP Transistor

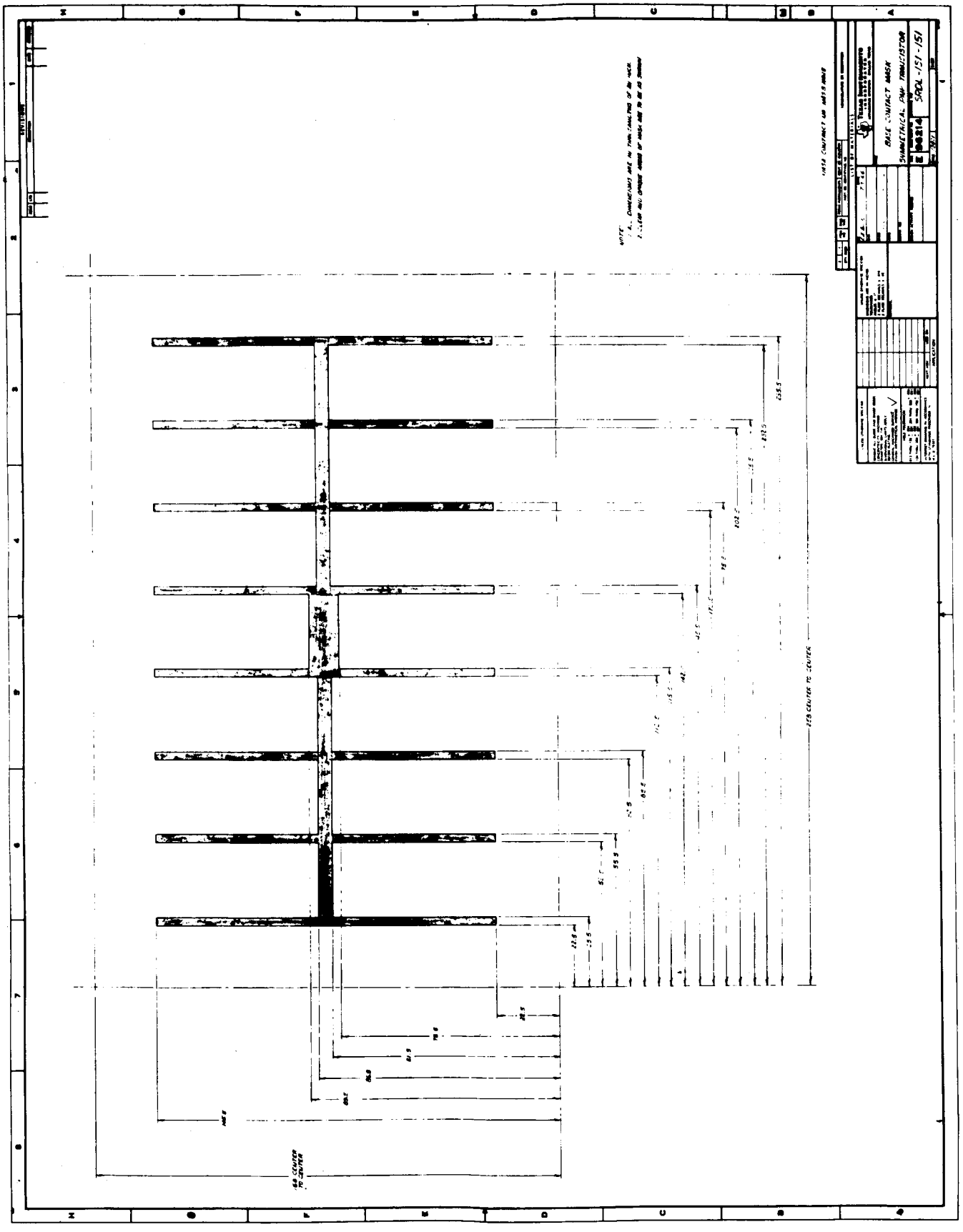


Figure 24. Base Contact Mask, Symmetrical PNP Transistor

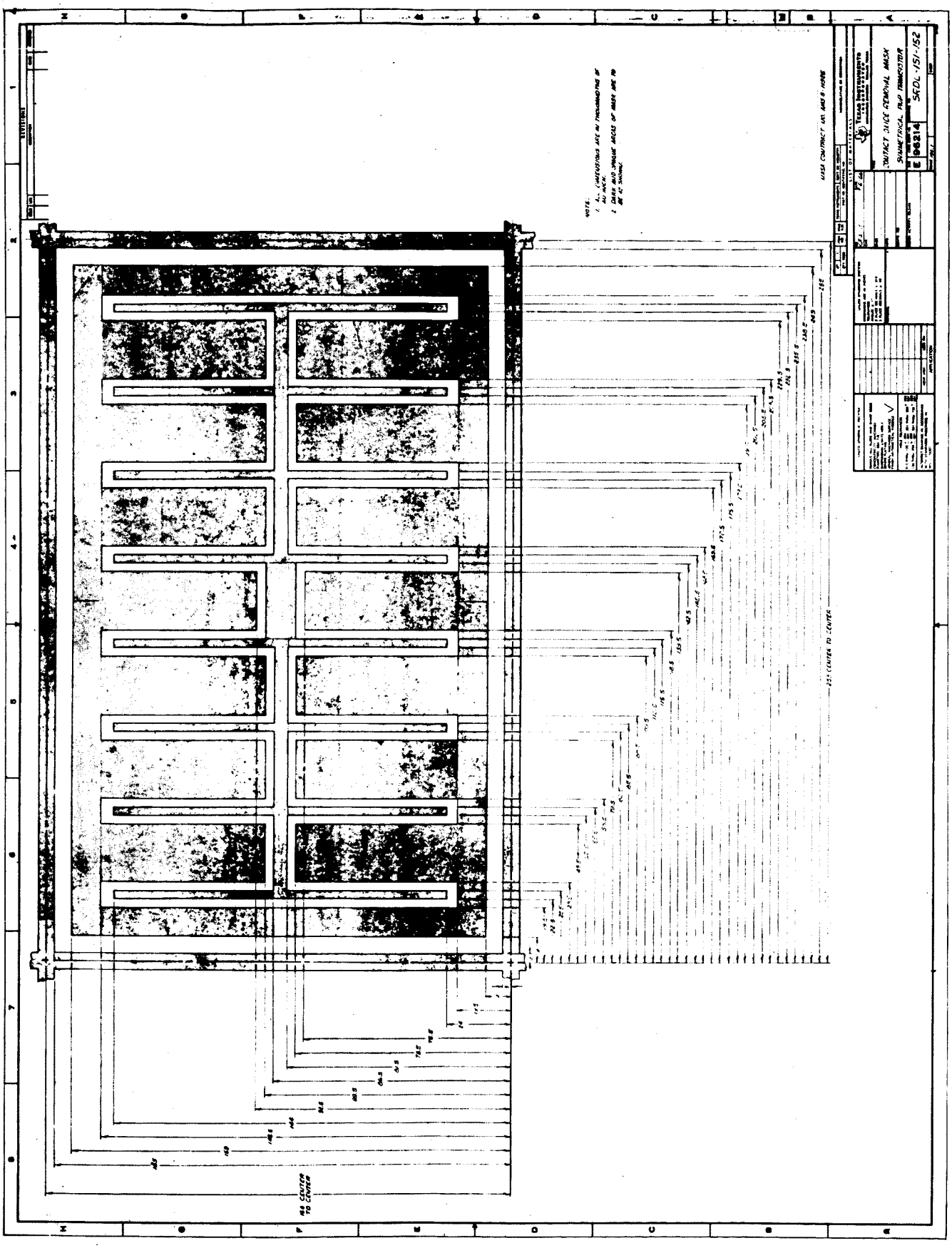


Figure 25. Contact Oxide Removal Mask, Symmetrical PNP Transistor

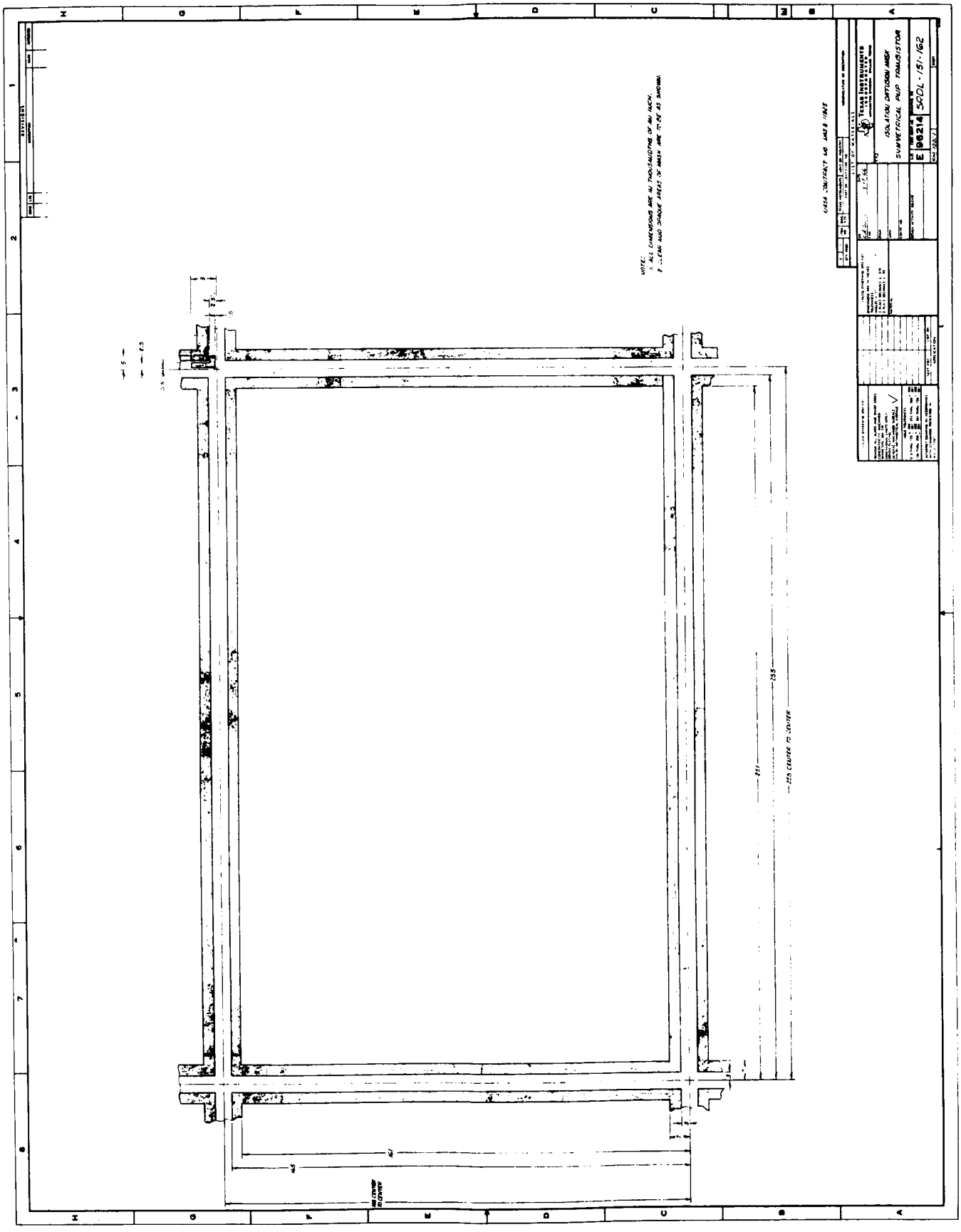


Figure 26. Isolation Diffusion Mask, Symmetrical PNP Transistor

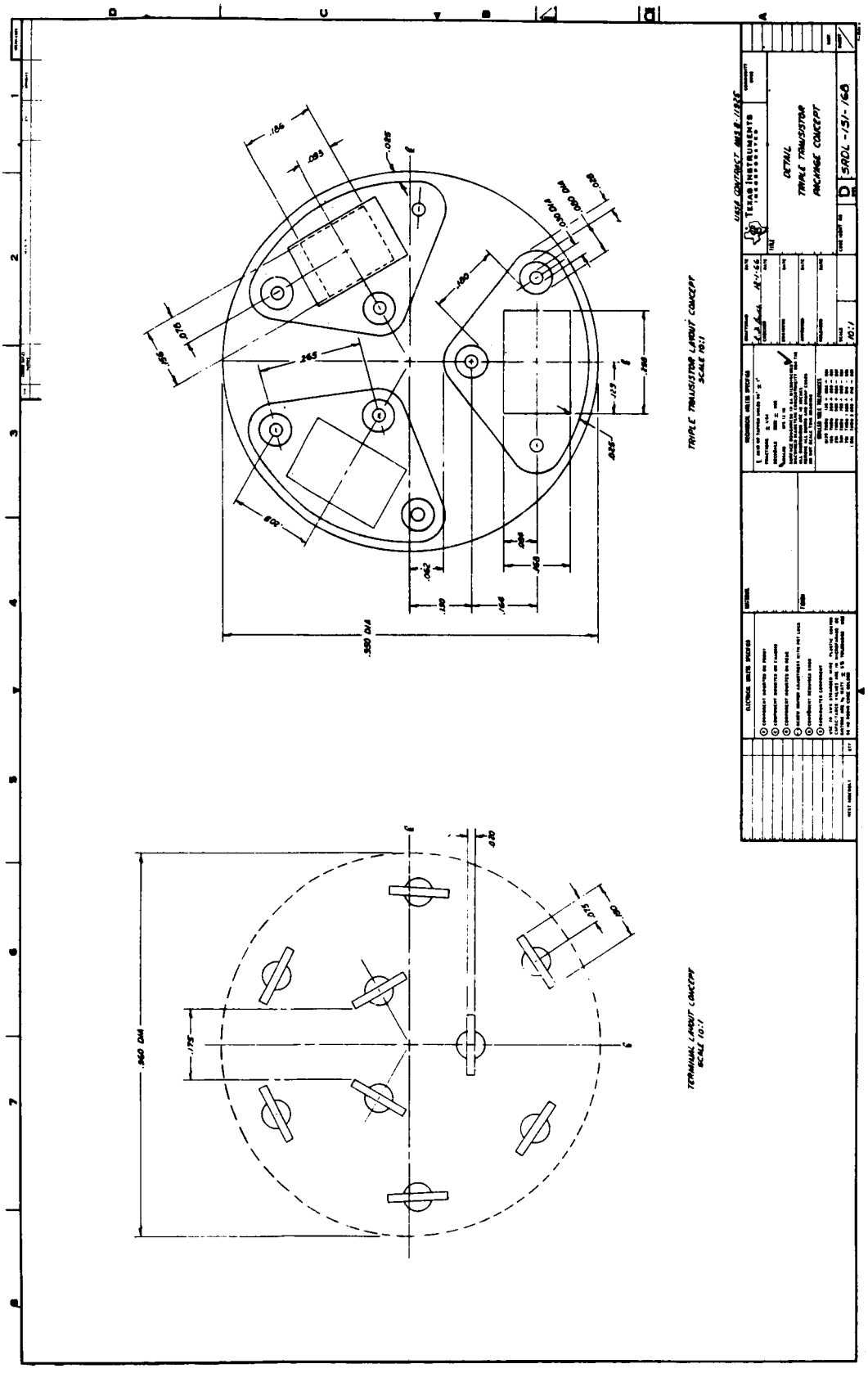


Figure 27. Detail, Triple Transistor Package Concept

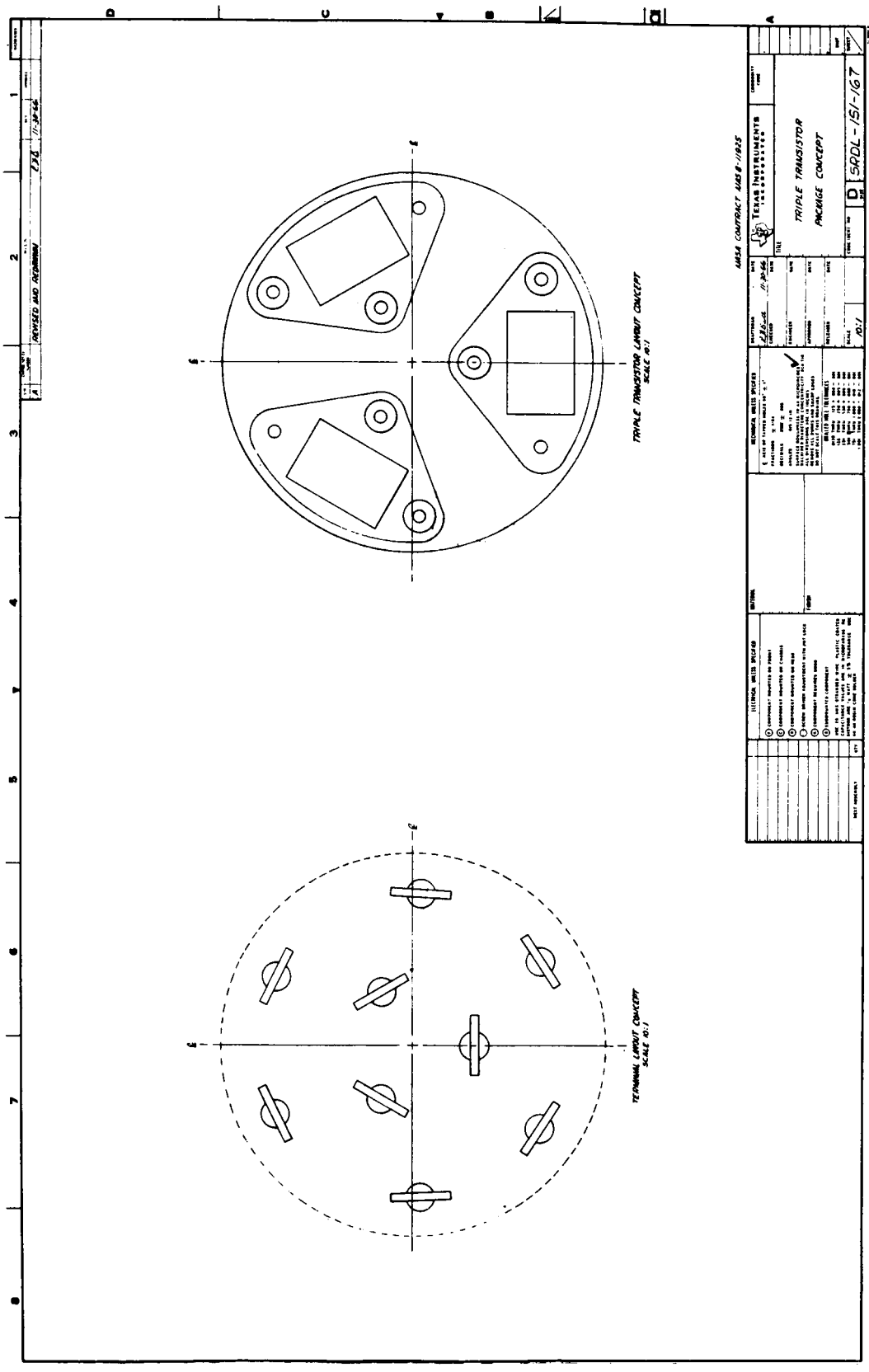


Figure 28. Triple Transistor Package Concept

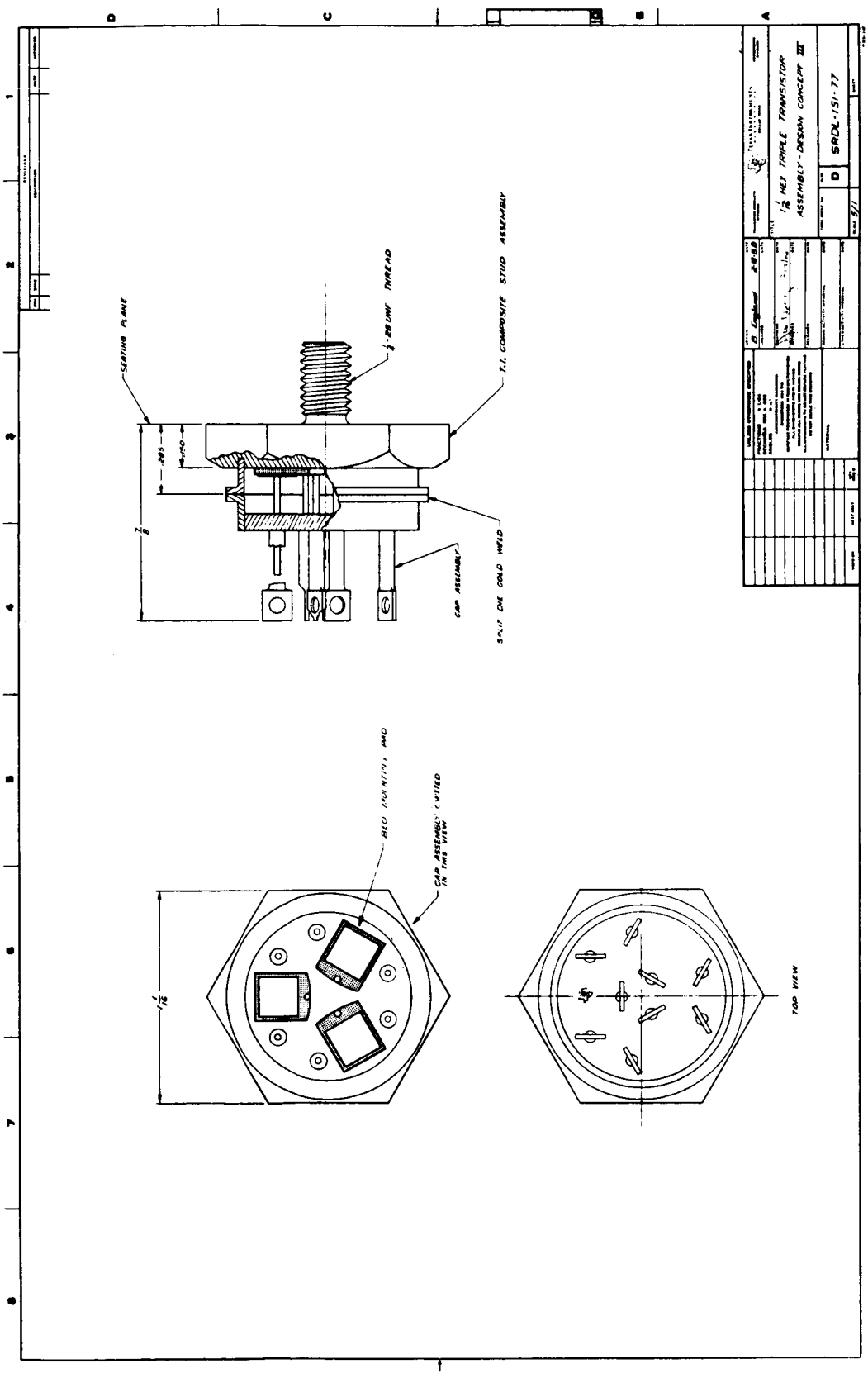


Figure 29. 1-1/16 Hex Triple Transistor Assembly: Design Concept III

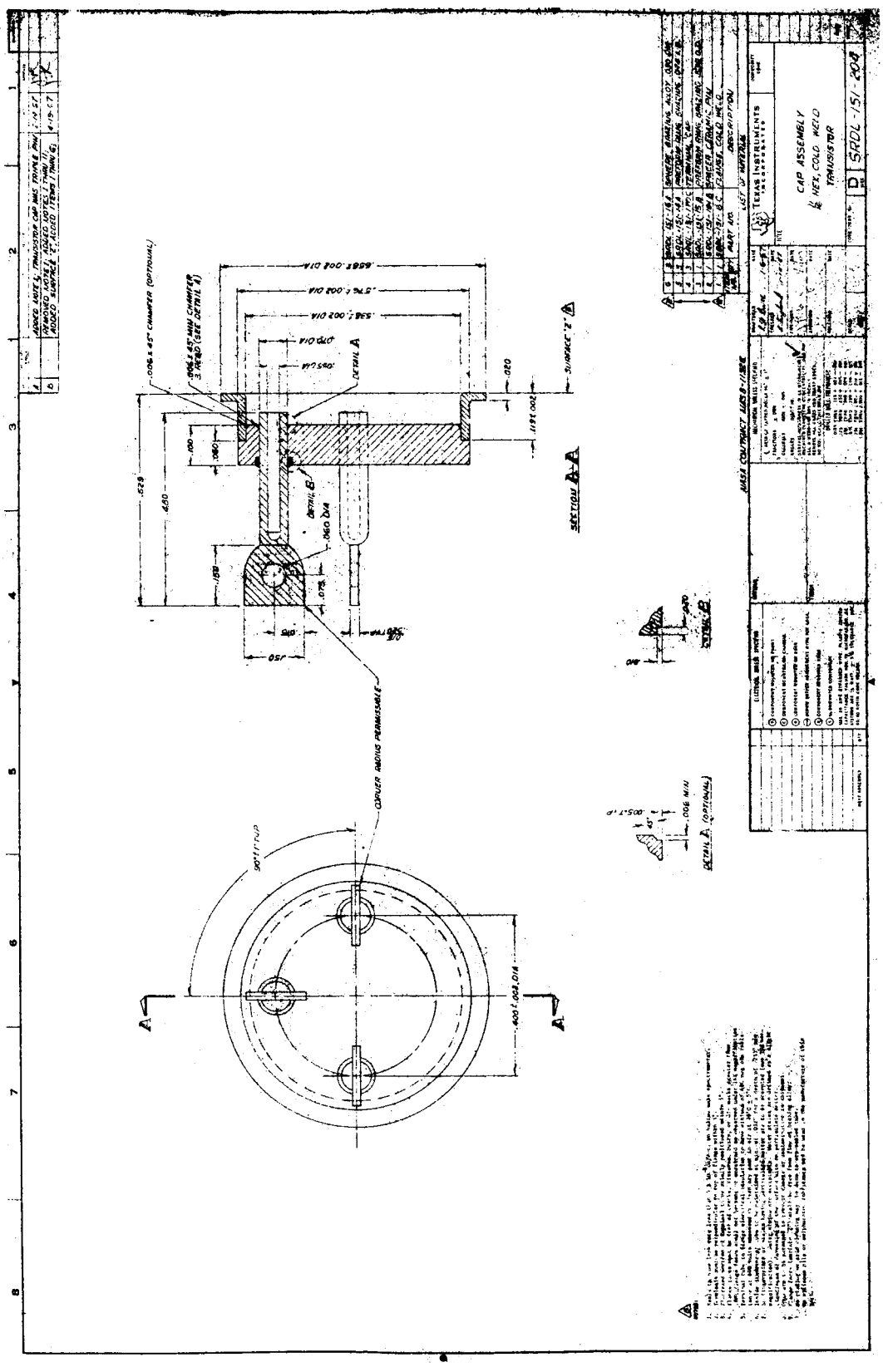


Figure 30. Cap Assembly, 11/16 Hex, Cold Weld Transistor

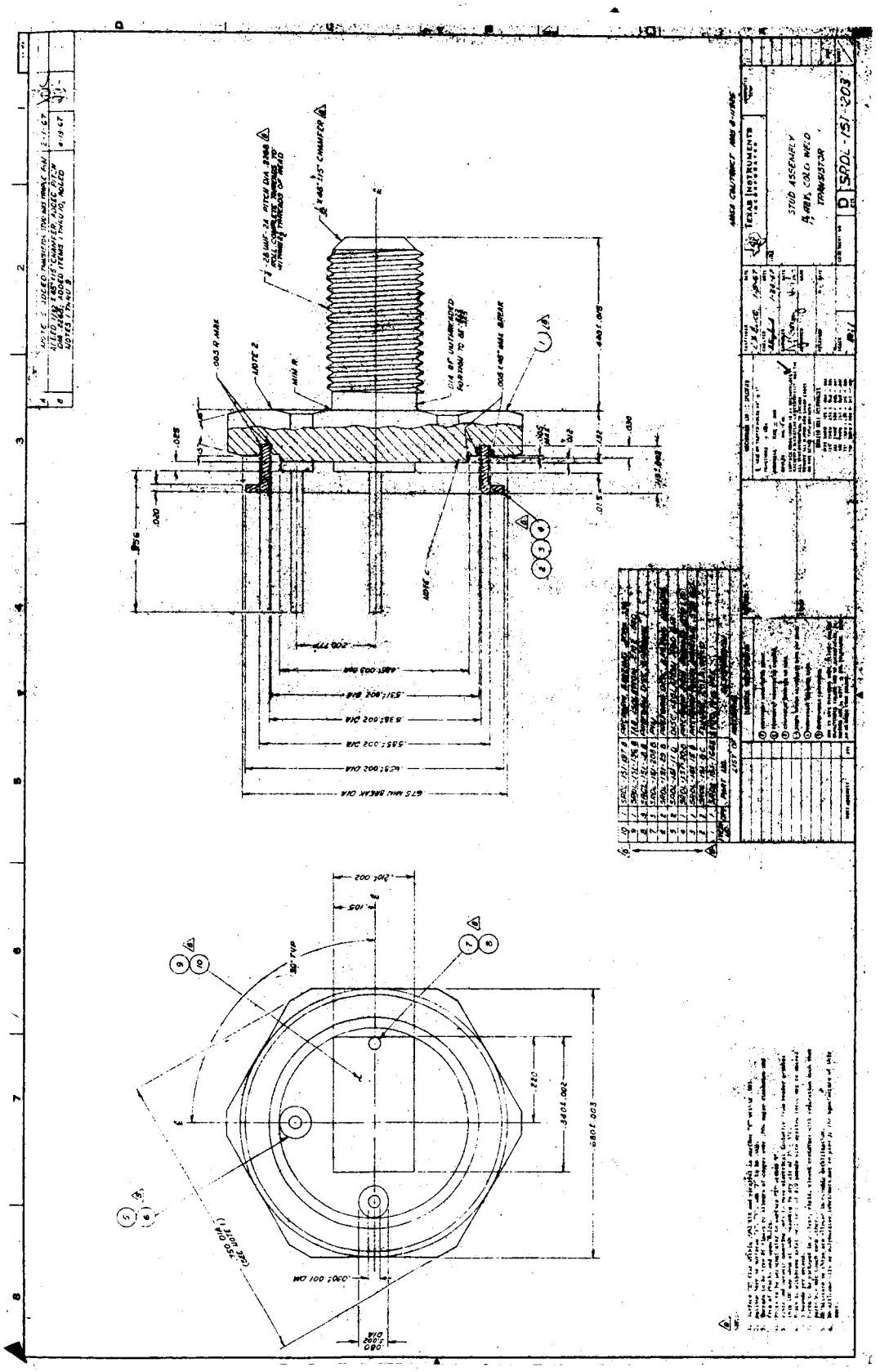


Figure 31. Stud Assembly, 11/16 Hex, Cold Weld Transistor

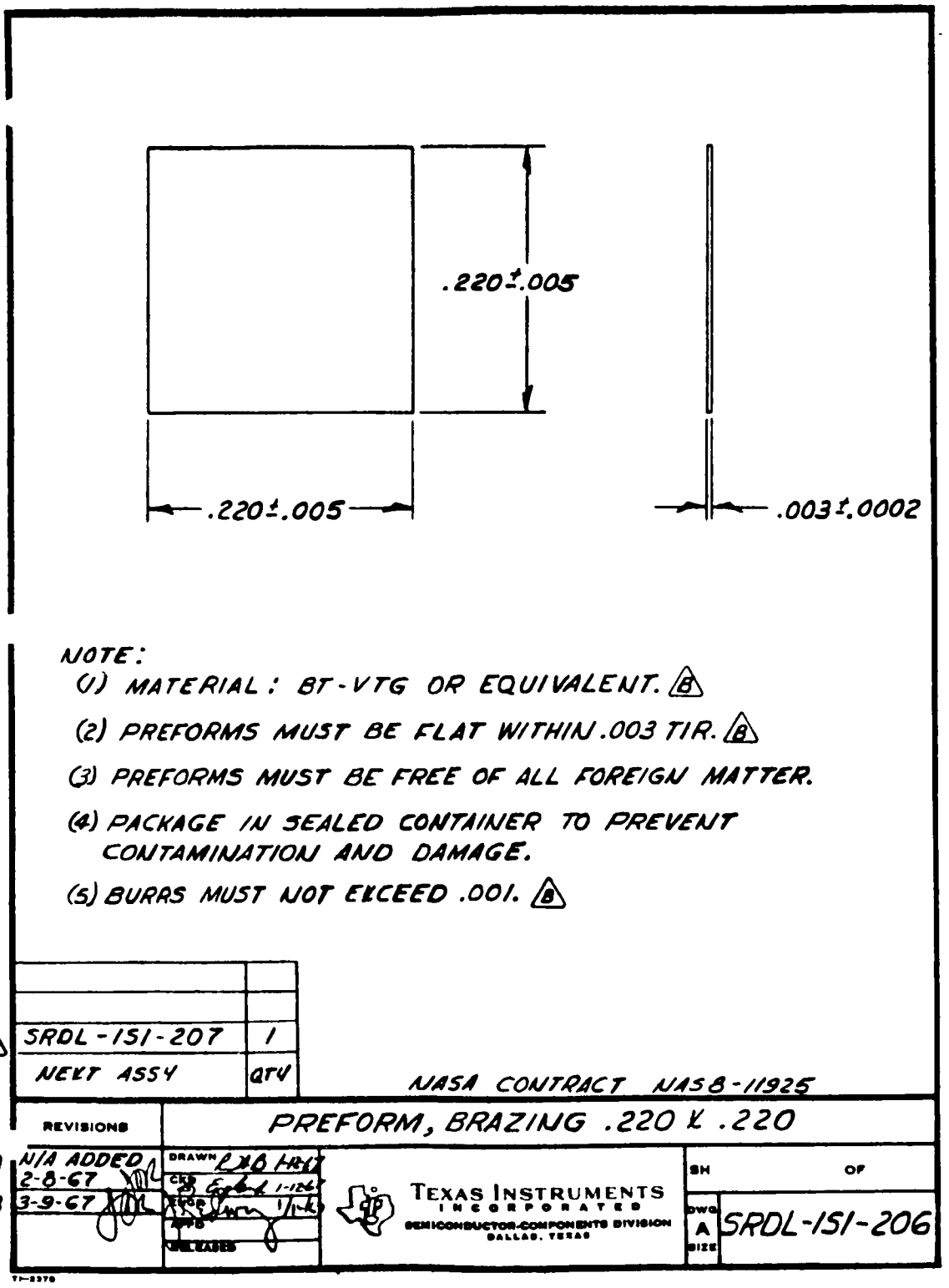


Figure 32. Brazing Preform, 0.220 inch by 0.220 inch

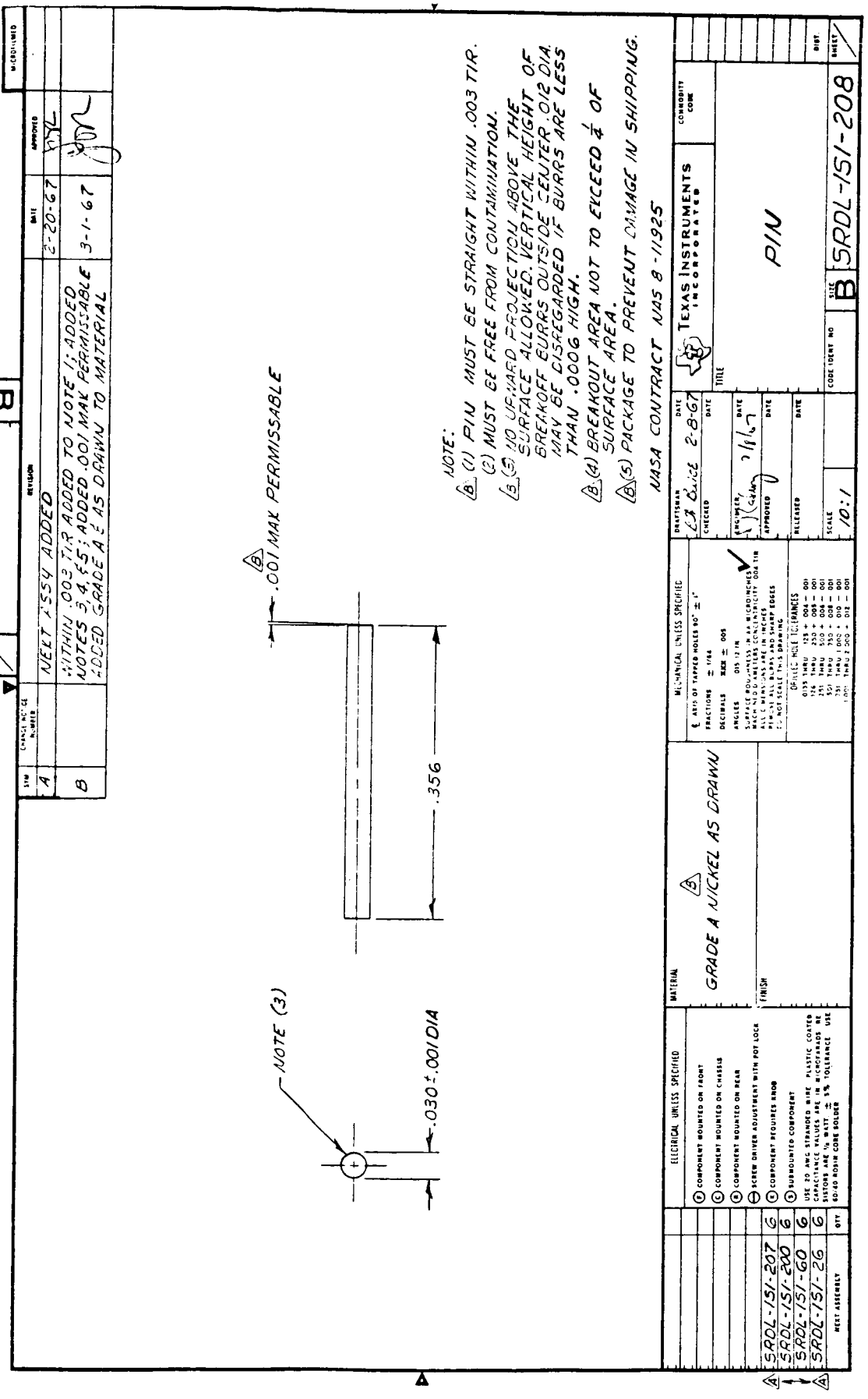
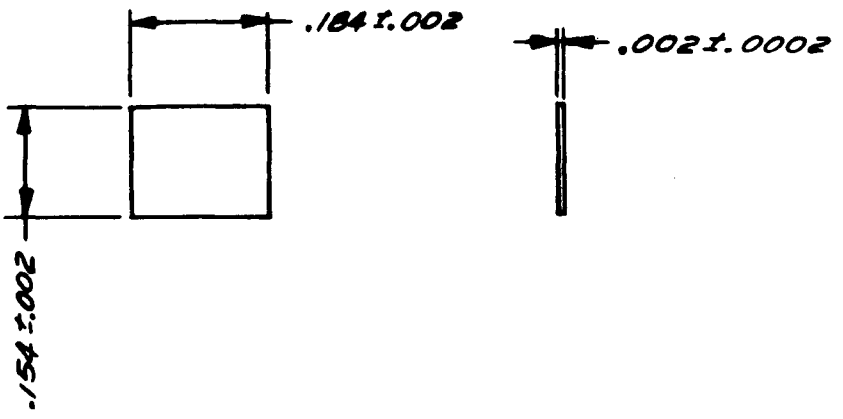


Figure 33. Pin



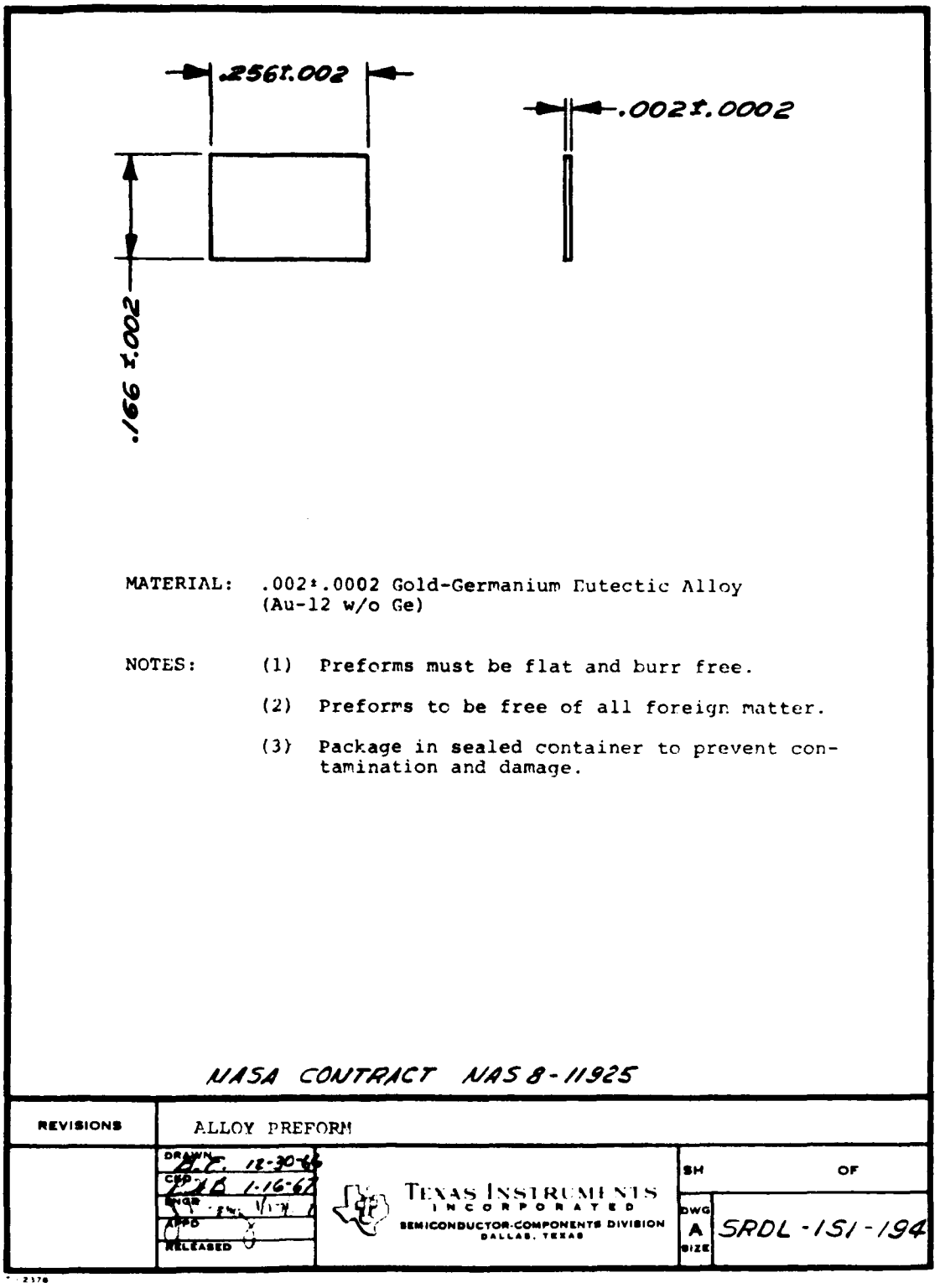
MATERIAL: .002 ± .0002 Gold-Germanium Eutectic Alloy (Au-12 w/o Ge)

NOTES:
(1) Preforms must be flat and burr free.
(2) Preforms to be free of all foreign matter.
(3) Package in sealed container to prevent contamination and damage.

NASA CONTRACT NAS 8-11925

REVISIONS	ALLOY PREFORM		
	DRAWN 12-30-66 CHKD 1-16-67 ENGR APPD RELEASED	TEXAS INSTRUMENTS INCORPORATED SEMICONDUCTOR-COMPONENTS DIVISION DALLAS, TEXAS	SH OF DWG A SIZE SRDL-151-195

Figure 34. Alloy Preform



MATERIAL: .002±.0002 Gold-Germanium Eutectic Alloy (Au-12 w/o Ge)

NOTES:
(1) Preforms must be flat and burr free.
(2) Preforms to be free of all foreign matter.
(3) Package in sealed container to prevent contamination and damage.

NASA CONTRACT NAS 8-11925

REVISIONS	ALLOY PREFORM		
	DRAWN H.E. 12-30-66 CHD [illegible] 1-16-67 ENGR APPD RELEASED	TEXAS INSTRUMENTS INCORPORATED SEMICONDUCTOR-COMPONENTS DIVISION DALLAS, TEXAS	SH OF DWG A SIZE SRDL-151-194

Figure 35. Alloy Preform

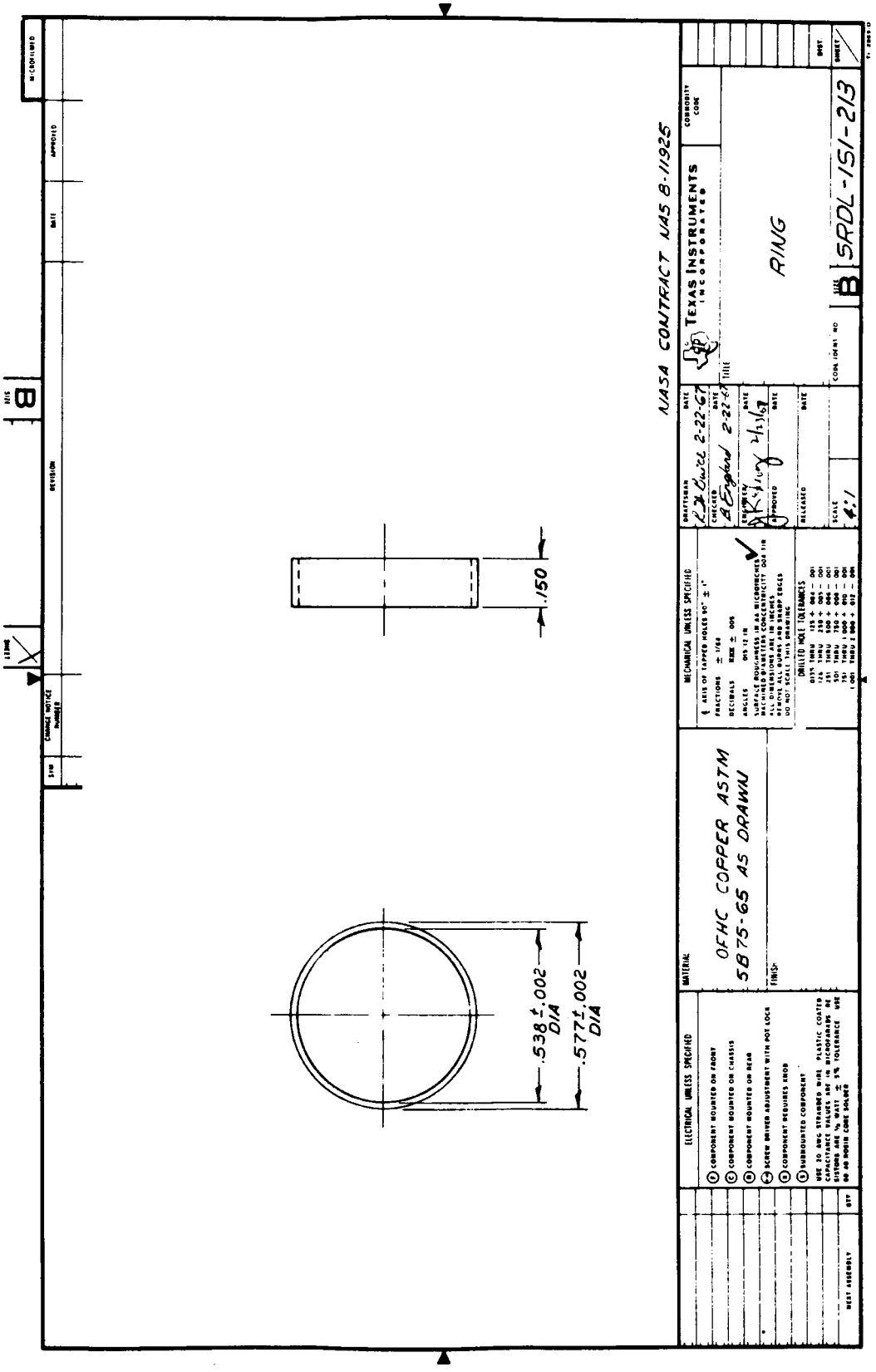


Figure 36. Ring

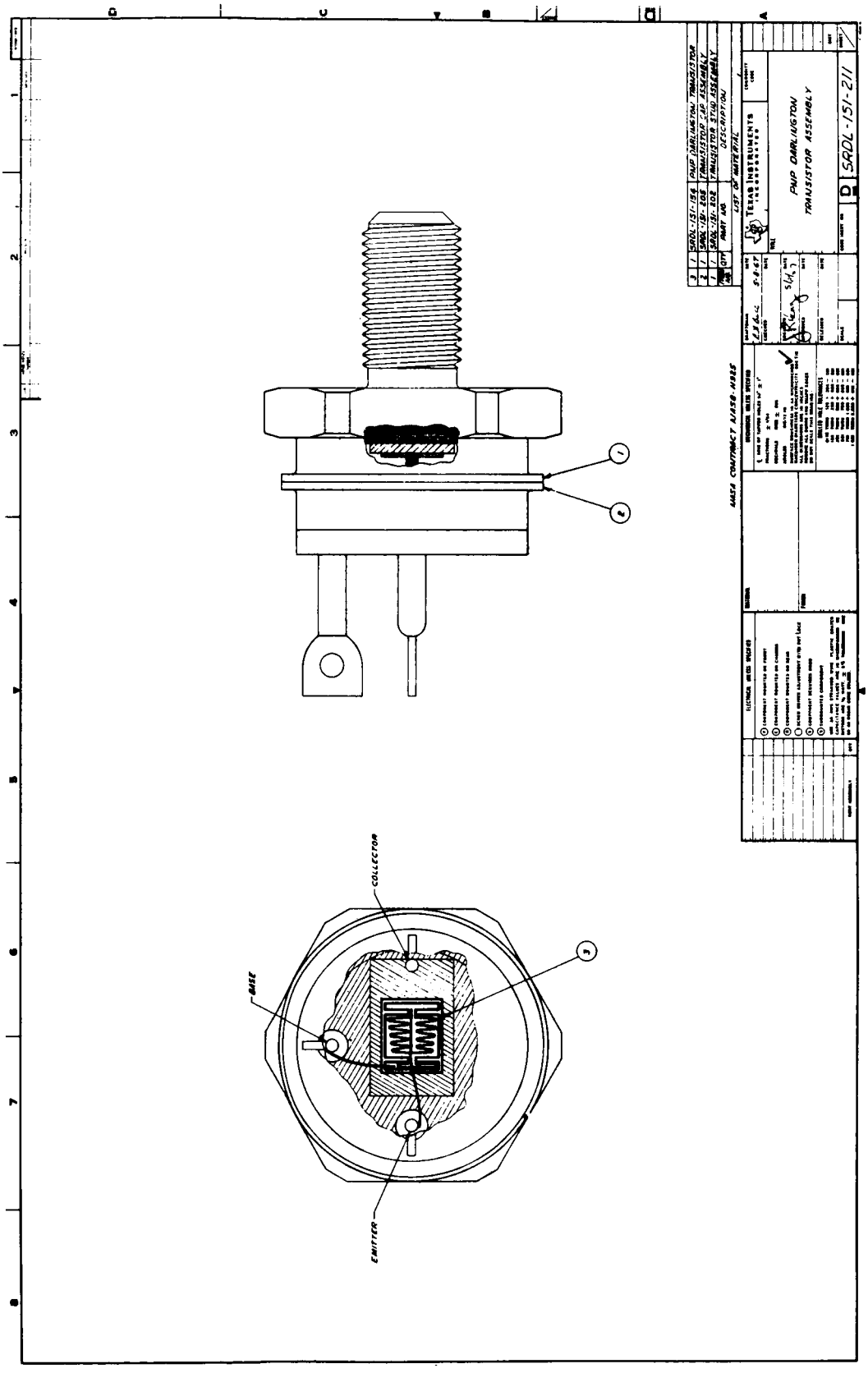


Figure 37. PNP Darlington Transistor Assembly

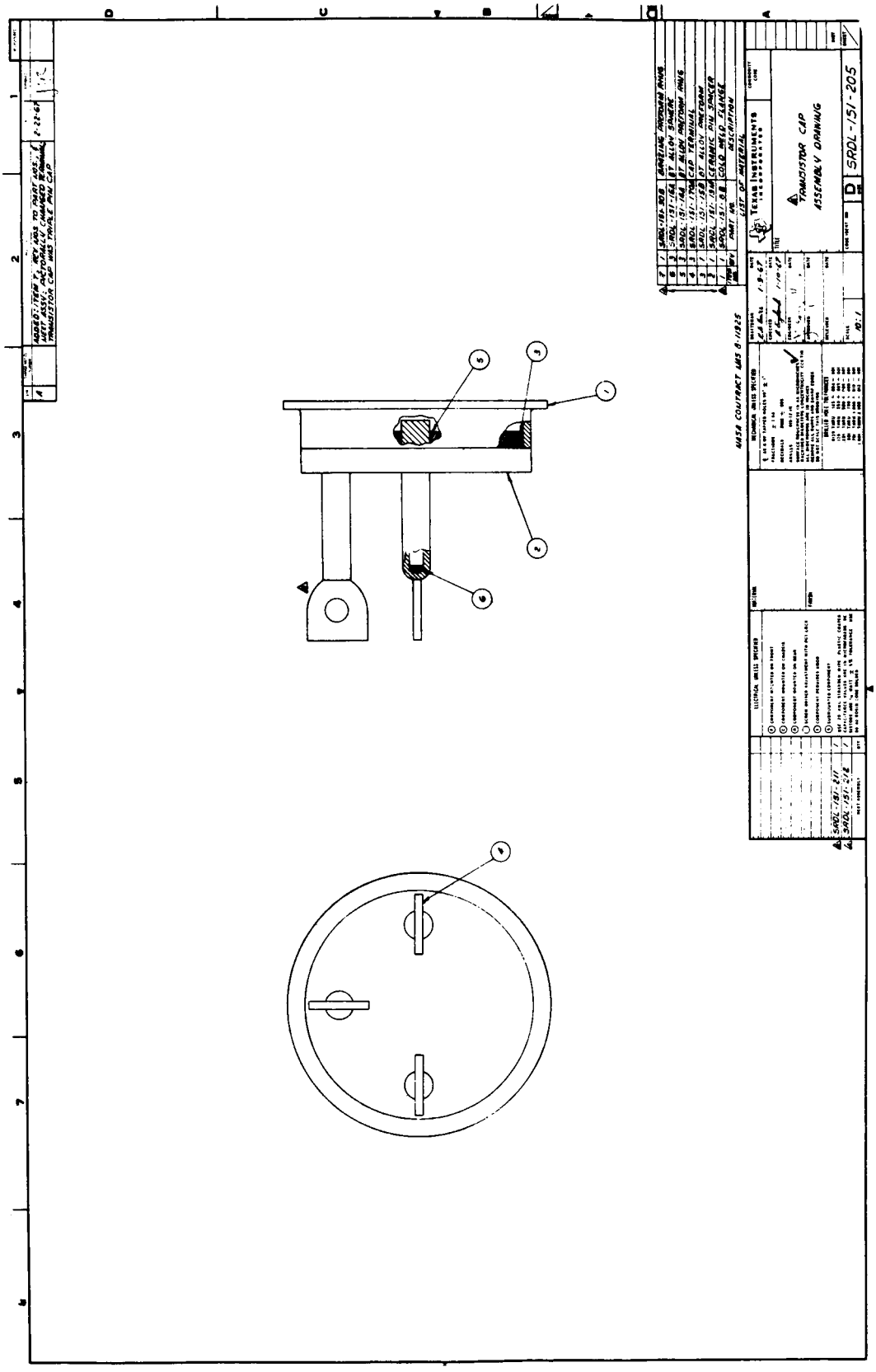


Figure 38. Triple Pin-Cap Assembly Drawing

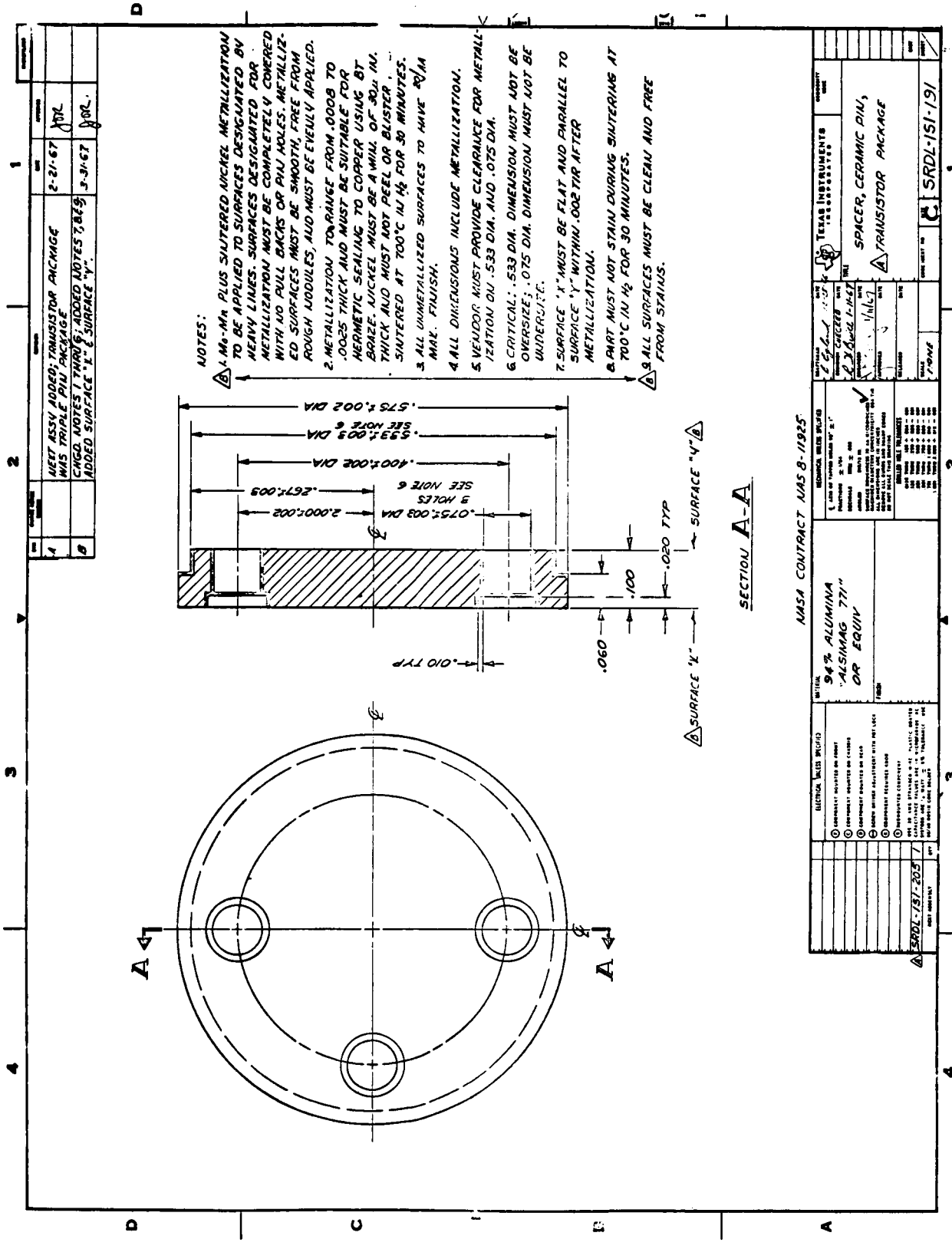


Figure 39. Transistor Package Ceramic Pin Spacer

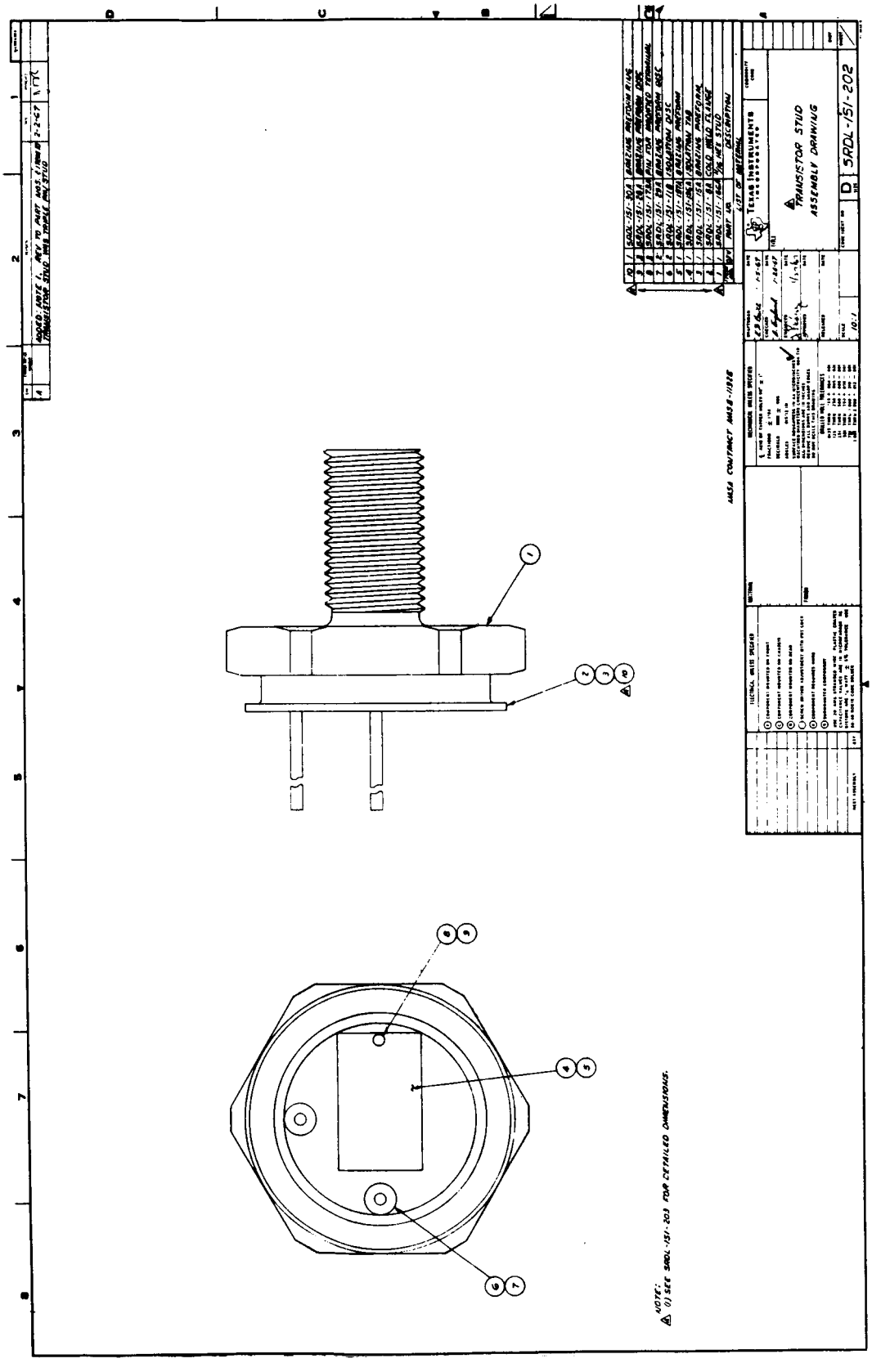


Figure 40. Transistor Stud Assembly Drawing

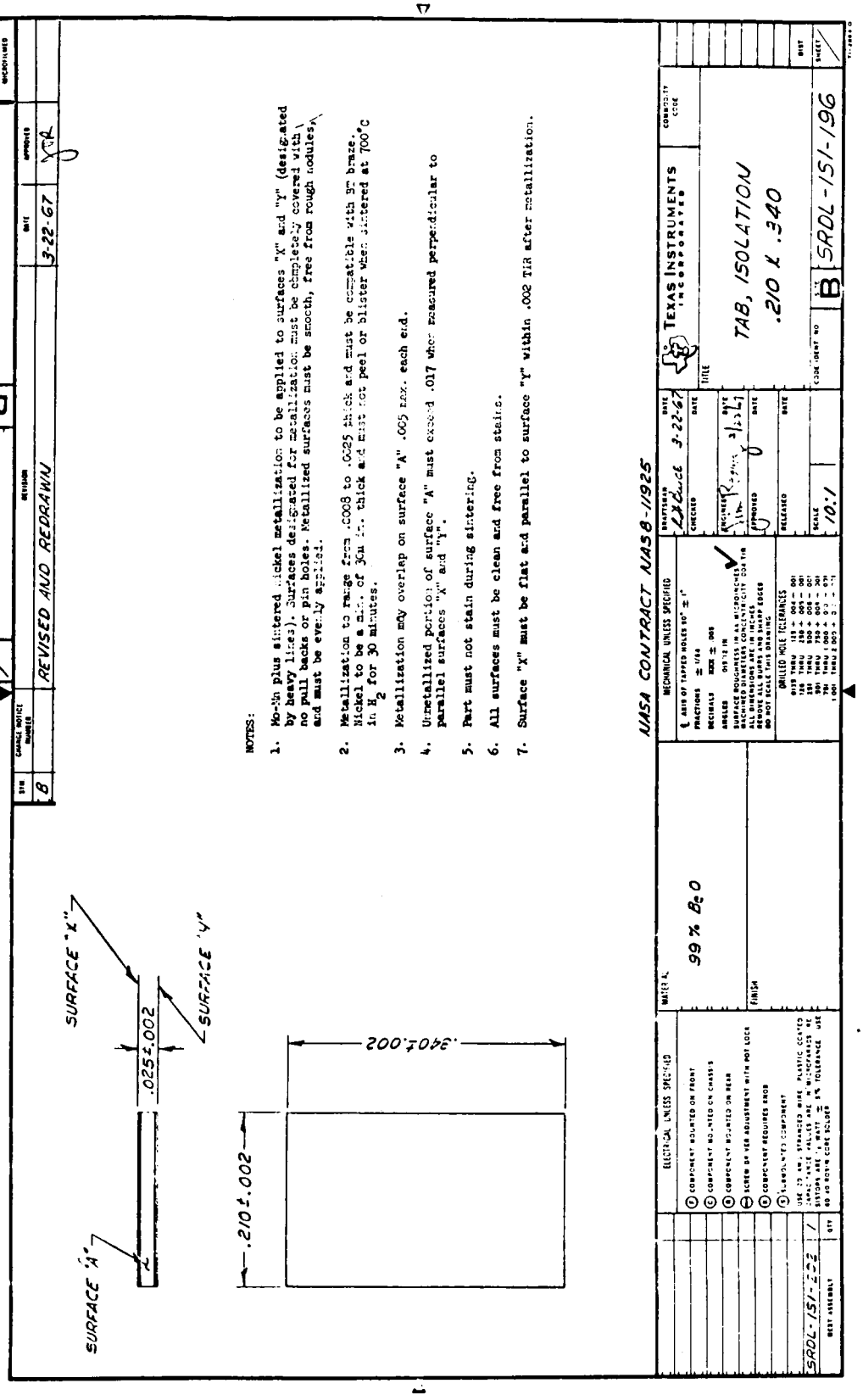


Figure 41. Isolation Tab, 0.210 in. by 0.340 in.

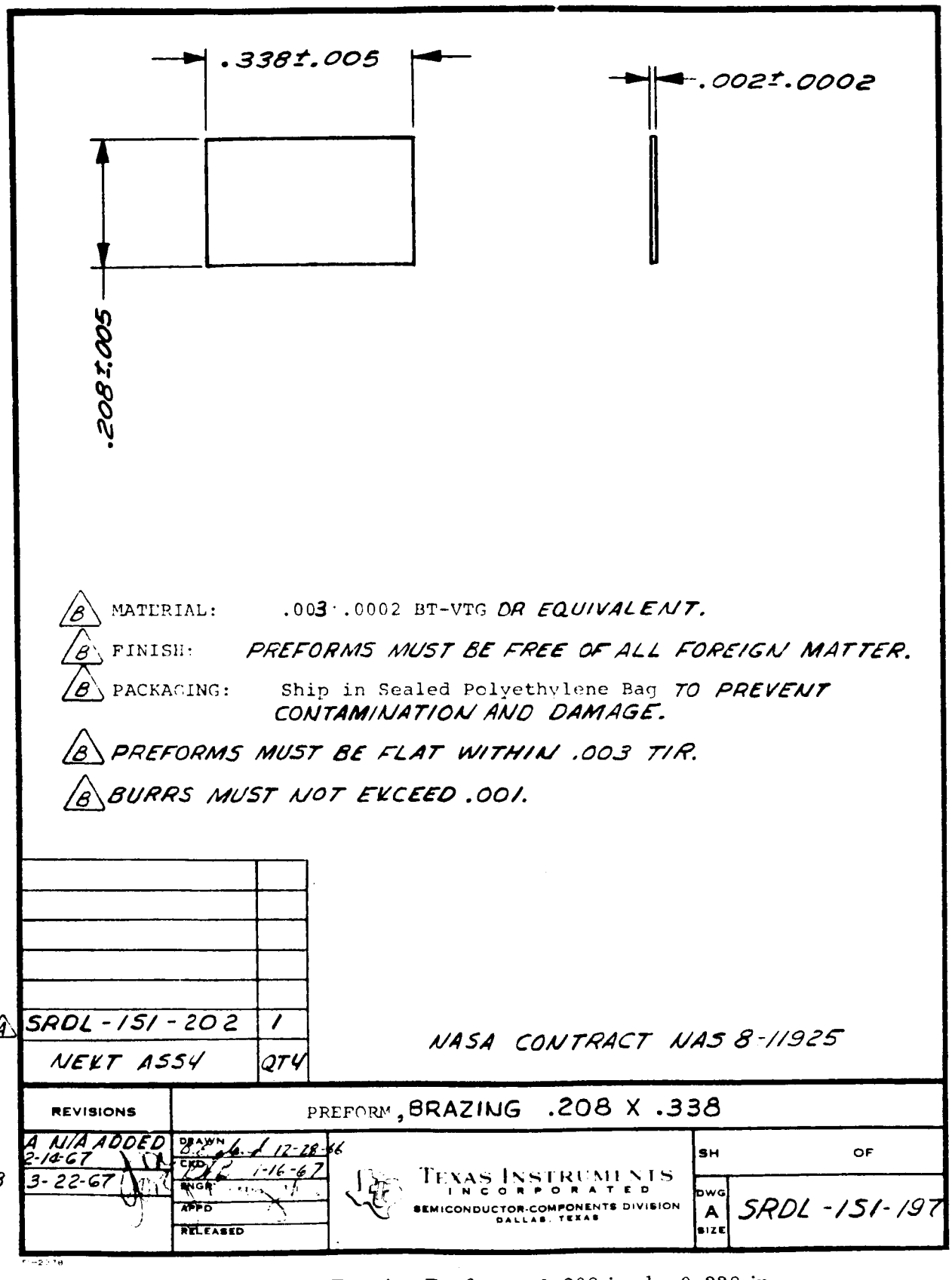


Figure 42. Brazing Preform, 0.208 in. by 0.338 in.

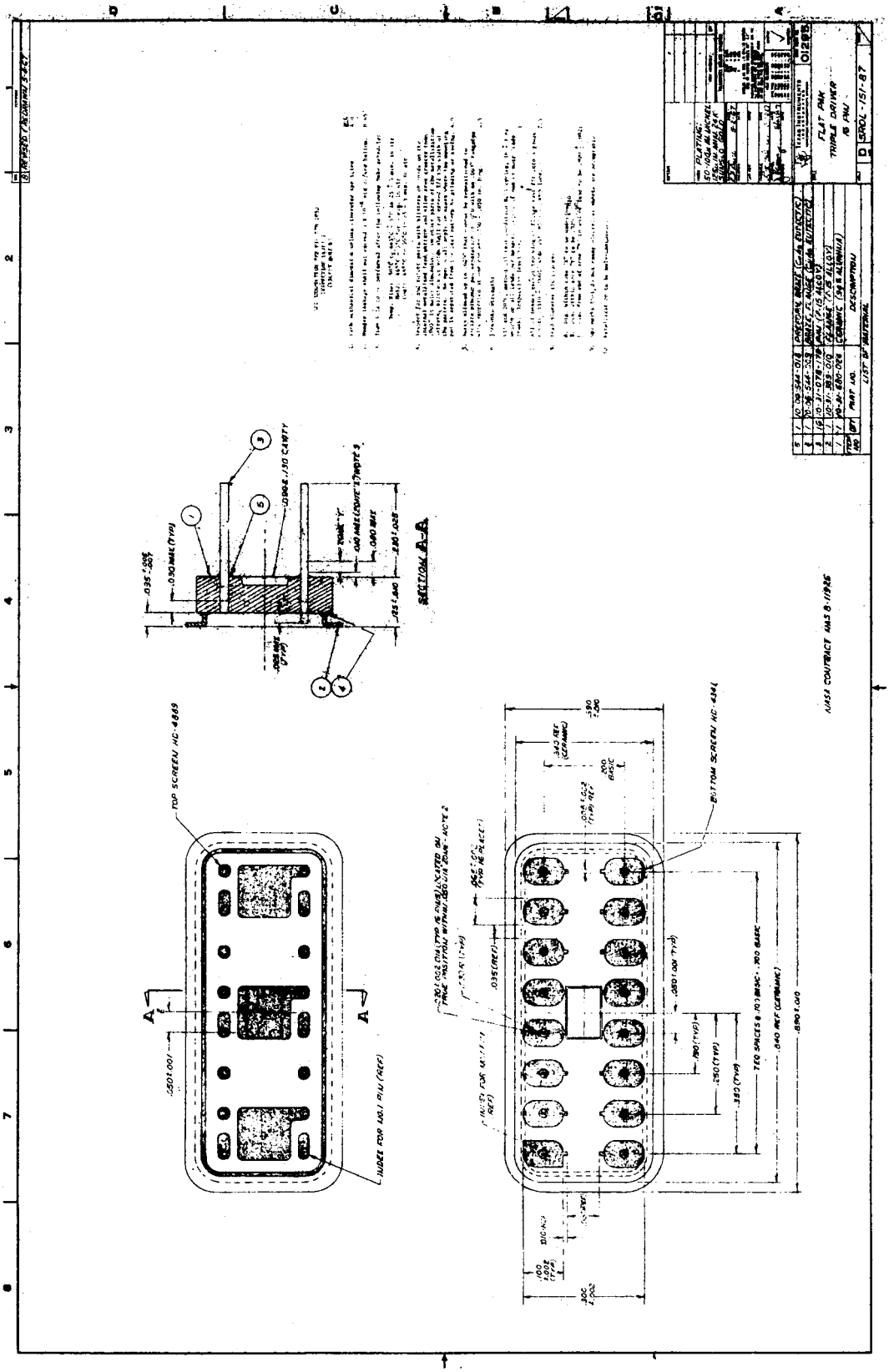


Figure 43. 16-Pin Triple Driver Flat Pak

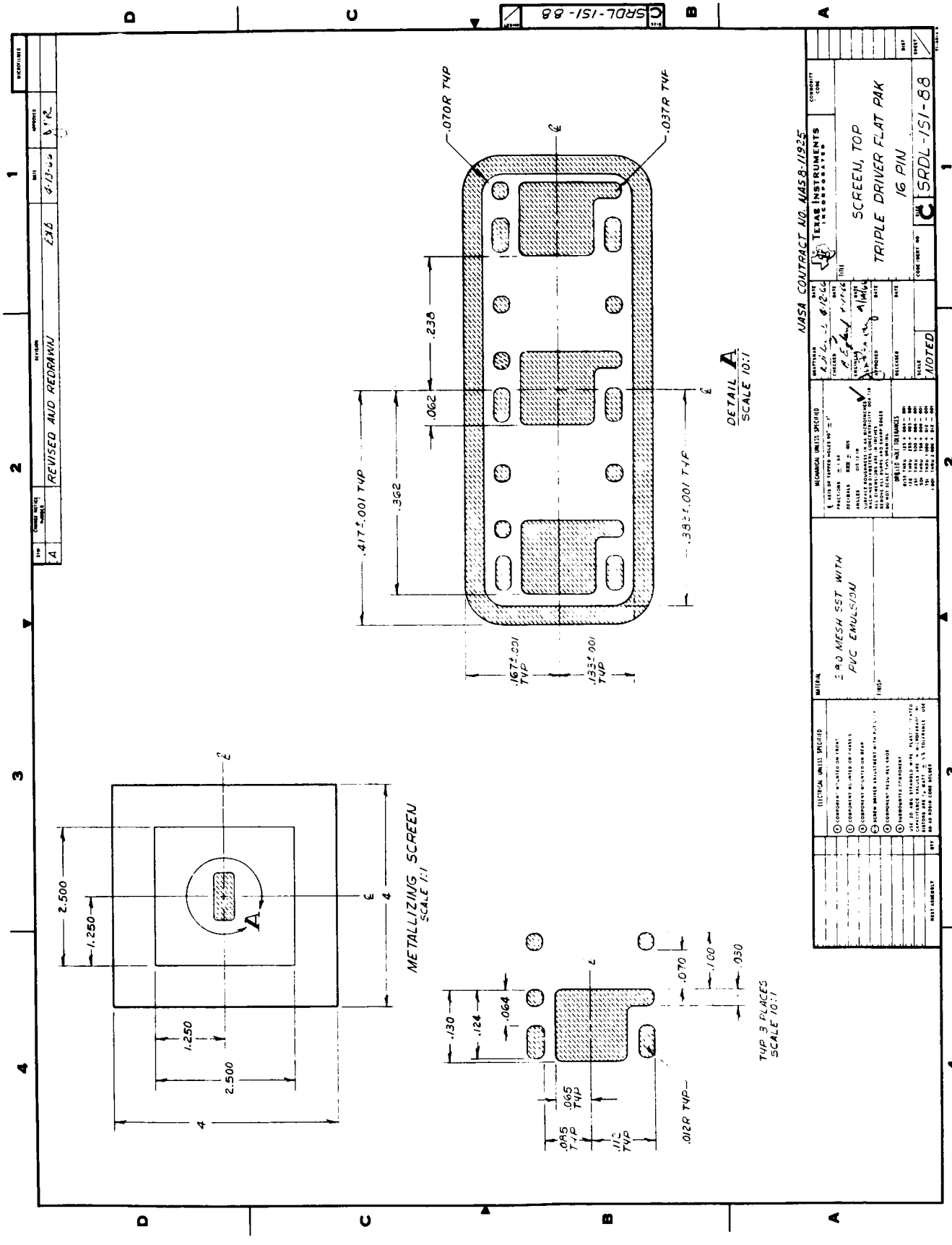


Figure 44. 16-Pin Triple Driver Flat Pak Top Screen

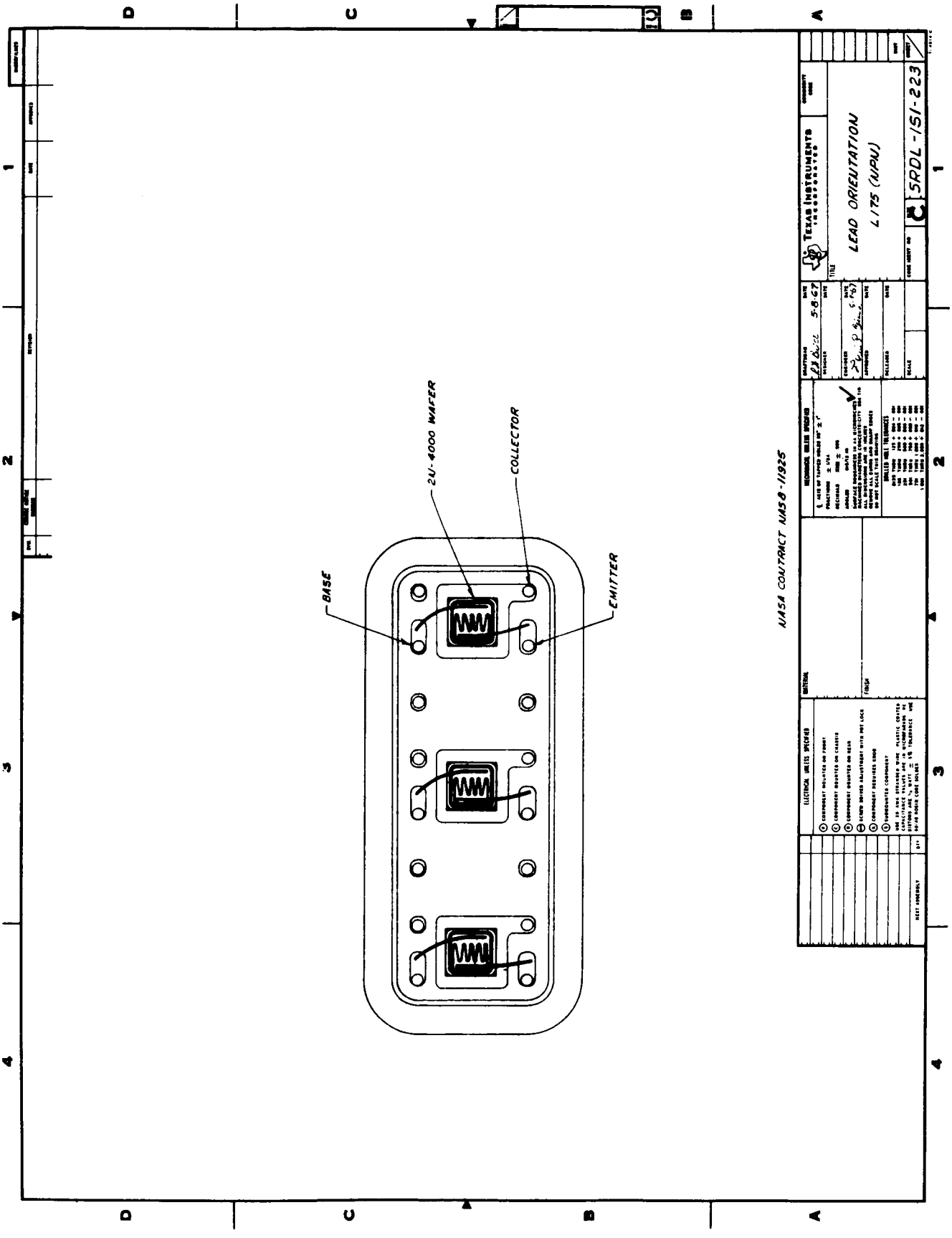


Figure 45. Lead Orientation L-175 (NPN)